Lecture 26 - 6.012 Wrap-up

December 13, 2005

Contents:

1. 6.012 wrap-up

Announcements:

Final exam TA review session: December 16, 7:30-9:30 PM,

Final exam: December 19, 1:30-4:30 PM, duPont; open book, calculator required; entire subject under examination but emphasis on lectures #19-26.
1. Wrap up of 6.012

- The amazing properties of Si

- two types of carriers: electrons and holes
  - however, can make good electronic devices with just one, i.e. MESFET (Metal-Semiconductor Field-Effect Transistor), or HEMT (High Electron Mobility Transistor)
  - but, can’t do complementary logic (i.e. CMOS) without two
• carrier concentrations can be controlled by addition of dopants
  – over many orders of magnitude (about $20!$)
  – and in short length scales ($nm$ range)

37 nm gate length MOSFET from Intel (IEDM ’05)
• carrier concentrations can be controlled electrostatically over many orders of magnitude (easily 10!)
• carriers are fast:
  - electrons can cross $L = 0.1 \, \mu m$ in about:
    $$\tau = \frac{L}{v_e} = \frac{0.1 \, \mu m}{10^7 \, cm/s} = 1 \, ps$$
  - high current density:
    $$J_e = qnv_e = 1.6 \times 10^{-19} \, C \times 10^{17} \, cm^{-3} \times 10^7 \, cm/s$$
    $$= 1.6 \times 10^5 \, A/cm^2$$
    \Rightarrow high current drivability to capacitance ratio
• extraordinary physical and chemical properties
  - can control doping over 8 orders of magnitude (p type and n type)
  - can make very low resistance ohmic contacts
  - can effectively isolate devices by means of pn junctions, trenches and SOI
The amazing properties of Si MOSFET

- ideal properties of Si/SiO₂ interface:
  - can drive surface all the way from accumulation to inversion (carrier density modulation over 16 orders of magnitude)
  - not possible in GaAs, for example
• performance improves as MOSFET scales down in size; as \( L, W \downarrow \):

- current:

\[
I_D = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_T)^2 \quad \text{unchanged}
\]

- capacitance:

\[
C_{gs} = WLC_{ox} \downarrow \downarrow
\]

- figure of merit for device switching delay:

\[
\frac{C_{gs} V_{DD}}{I_D} = L^2 \frac{2V_{DD}}{\mu (V_{GS} - V_T)^2} \downarrow \downarrow
\]

• No gate current.

• \( V_T \) can be engineered.

• MOSFETs come in two types: NMOS and PMOS.

• Easy to integrate.
The amazing properties of Si CMOS

- Rail-to-rail logic: logic levels are 0 and $V_{DD}$.
- No power consumption while idling in any logic state.
- Scales well.

As $L, W \downarrow$:

- Power consumption (all dynamic):

$$P_{\text{diss}} = fC_L V_{DD}^2 \propto fWLC_{ox}V_{DD}^2 \downarrow\downarrow$$

- Propagation delay:

$$t_P \propto \frac{C_L V_{DD}}{W \mu C_{ox}(V_{DD} - V_T)^2} \downarrow\downarrow$$

- Logic density:

$$\text{Density} \propto \frac{1}{A} = \frac{1}{WL} \uparrow\uparrow$$
Transistor density continues to double every 2 years.

INTEL 6-T SRAM CELL SIZE TREND

Figure by MIT OCW.
Figure by MIT OCW.
MOSFET scaling

Straight MOSFET scaling doesn’t work.

- Electric field increases
  \[ E_y \approx \frac{V_{DD}}{L} \uparrow \]

- Power density increases
  \[ \frac{P_{diss}}{\text{device area}} \propto \frac{fWL C_{ox} V_{DD}^2}{WL} = f C_{ox} V_{DD}^2 \]

But

\[ t_P \downarrow \downarrow \Rightarrow f \uparrow \uparrow \Rightarrow \frac{P_{diss}}{\text{device area}} \uparrow \uparrow \Rightarrow T \uparrow \uparrow \]
• total power increases

Figure by MIT OCW.
⇒ must scale $V_{DD}$
Where is this going?

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The future of microelectronics according to Intel:

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Exciting times ahead in Si IC technology:

- **analog electronics** (since ~ 50′s): amplifiers, mixers, oscillators, DAC, ADC, etc.
- **digital electronics** (since ~ 60′s): computers, microcontrollers, random logic, DSP
- **solid-state memory** (since ~ 60′s): dynamic random-access memory, flash
- **energy conversion** (since ~ 70′s): solar cells
- **power control** (since ~ 70′s): ”smart” power
- **communications** (since ~ 80′s): VHF, UHF, RF front ends, modems, fiber-optic systems
- **sensing, imaging** (since ~ 80′s): photodetectors, CCD cameras, CMOS cameras, many kinds of sensors
- **micro-electro-mechanical systems** (since ~ 90′s): accelerometers, movable mirror displays
- **biochip** (from ~ 2000): DNA sequencing, μfluidics
- **vacuum microelectronics** (from ~ 2000?): field-emitter displays
- ???? (microreactors, microturbines, etc.)

Lots of activity in other semiconductors:
- **GaN**: LEDs, high power, high f transistors
- **GaAs, InP**: lasers, detectors for fiber optics communication,
Circuit design lessons from 6.012:

1. Importance of optimum level of abstraction:

- device physics equations, *i.e.*:
  \[
  I_D = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_T)^2, \text{ etc.}
  \]

- device equivalent circuit models, *i.e.*:

- device SPICE models, *i.e.*:
2. Many considerations in circuit design:

- multiple performance specs:
  - in analog systems: gain, bandwidth, power consumption, swing, noise, etc.
  - in digital systems: propagation delay, power, ease of logic synthesis, noise, etc.

- need to be immune to temperature variations and device parameter variations (i.e.: differential amplifier)

- must choose suitable technology: CMOS, BJT, CBJT, BiCMOS, etc.

- must avoid costly components (i.e.: resistors, capacitors)

3. Trade-offs:

- gain-bandwidth trade-off in amplifiers (i.e.: Miller effect)

- performance-power trade-off (i.e.: delay in logic circuits, gain in amplifiers)

- performance-cost trade-off (cost=design complexity, Si area, more aggressive technology)

- accuracy-complexity trade-off in modeling
Exciting times ahead in circuit design too:

- Numbers of transistors available outstrips ability to design by 3 to 1!
- Operational frequency of logic, analog, and communications circuits increasing very fast.
- Operational voltage shrinking quickly.
- New device technologies: GaAs HEMT, InP HBT, GaN HEMT, etc
More subjects in microelectronics at MIT


