• Announcements
  Final Exam - Tuesday, Dec 15, 9:00 am - 12 noon

• Review - Shunt feedback capacitances: $C_\mu$ and $C_{gd}$
  Miller effect: any C bridging a gain stage looks bigger at the input
  Marvelous cascode: CE/S-CB/G (E/SF-CB/G work, too - see $\mu$A741)
    large bandwidth, large output resistance
    used in gain stages and in current sources

  Using the Miller effect to advantage: Stabilizing OP Amps - the $\mu$A741

• Intrinsic high frequency limitations of transistors
  General approach
  MOSFETs: $f_T$
    biasing for speed
    impact of velocity saturation
    design lessons

  BJT$\text{s}$: $f_\beta$, $f_T$, $f_\alpha$
    biasing for speed
    design lessons
Summary of OCTC and SCTC results

- **OCTC**: an estimate for $\omega_{HI}$
  1. $\omega_{HI}^*$ is a weighted sum of $\omega$'s associated with *device capacitances*:
     (add RC's and invert)
  2. Smallest $\omega$ (largest RC) dominates $\omega_{HI}^*$
  3. Provides a lower bound on $\omega_{HI}$

- **SCTC**: an estimate for $\omega_{LO}$
  1. $\omega_{LO}^*$ is a weighted sum of $\omega$'s associated with *bias capacitors*:
     (add $\omega$'s directly)
  2. Largest $\omega$ (smallest RC) dominates $\omega_{LO}^*$
  3. Provides a upper bound on $\omega_{LO}$

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The Miller effect (general)

Consider an amplifier shunted by a capacitor, and consider how the capacitor looks at the input and output terminals:

\[ v_{\text{in}} (1-A_v) v_{\text{in}} C_m v_{\text{out}} = A_v v_{\text{in}} \]

Consider an amplifier shunted by a capacitor, and consider how the capacitor looks at the input and output terminals:

\[ i_{\text{in}} = C_m \frac{d[(1-A_v)v_{\text{in}}]}{dt} = (1-A_v)C_m \frac{dv_{\text{in}}}{dt} \]

Note: \( A_v \) is negative

\[ C_{\text{in}} \approx (1-A_v)C_m \]

\[ C_{\text{out}} \approx C_m \]
The cascode when the substrate is grounded:
High frequency issues:

L.E.C. of cascode: can’t use equivalent transistor idea here because it didn’t address the issue of the C's!

Voltage gain ≈ -1 so minimal Miller effect.

Common-source gain without the Miller effect penalty!
Multi-stage amplifier analysis and design: The µA741

Figuring the circuit out:

- Emitter-follower/
  common-base "cascode"
  differential gain stage

- Darlington common-
  emitter gain stage

- Current mirror load

- Push-pull output

The full schematic

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Simplified schematic

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Multi-stage amplifier analysis and design: Understanding the µA741 input "cascode"

Begin with the BJT building-block stages:

1. Common base:
   - $r_t$ : input resistance
   - $g_{m,b}$ : transconductance

2. Common emitter:
   - $r_l = 1/g_l$
   - $g_{m,e}$ : medium
   - $g_o$ : small

3. Emitter follower:
   - $g_{m,f}$ : large
   - $g_{o,f}$ : small
   - $g_{t,f}$, $g_{i}$ : cannot generalize

Relative sizes:
- $g_m$: large
- $g_{\pi}$: medium
- $g_o$: small
- $g_t$, $g_i$: cannot generalize

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Lecture 24 - Slide 6
Multi-stage amplifier analysis and design: Two-port models

Two different "cascode" configurations, this time bipolar:

In a bipolar cascode, starting with an emitter follower still reduces the gain, but it also gives twice the input resistance, which is helpful.
Multi-stage amplifier analysis and design: MOSFET 2-port models

Reviewing our building-block stages:

Relative sizes:
- \( g_m, g_{mb} \): large
- \( g_o \): small
- \( g_t, g_l \): cannot generalize
Multi-stage amplifier analysis and design: Two-port models

Two different "cascode" configurations:

With MOSFETs, starting a cascode with a source follower costs a factor of two in gain because \( r_{out} \) for an SF is small, so it isn’t very attractive.
Multi-stage amplifier analysis and design: The µA741

The circuit: a full schematic

The monolithic capacitor made the µA741 "complete" and a big success. Why is it needed? What does it do?

C₁ is in a Miller position across Q₁₆
Multi-stage amplifier analysis and design: The µA741

Why is there a capacitor in the circuit?: the added capacitor introduces a low frequency pole that stabilizes the circuit.

Without it the gain is still greater than 1 when the phase shift exceeds 180° (dashed curve). This can result in positive feedback and instability.

With it the gain is less than 1 by the time the phase shift exceeds 180° (solid curve).
Intrinsic performance - the best we can do

We've focused on $\omega_{HI}$, the upper limit of mid-band, but even when $\omega > \omega_{HI}$ the $|A_v| > 1$, and the circuit is useful. For example, for the common source stage we had

$$A_v(j\omega) = \frac{-g_t (g_m - j\omega C_{gd})}{(j\omega)^2 C_{gs} C_{gd} + j\omega [(g_l + g_o) C_{gs} + (g_l + g_o + g_t + g_m) C_{gd} ] + (g_l + g_o) g_t}$$

A Bode plot of $A_v$ is shown to the right:

When we look for a metric to compare the ultimate performance limits of transistors, we make note of this and ask how high can a device in isolation have provide voltage or current gain?
Intrinsic performance - the best we can do, cont.

Consider the two possibilities shown below, one for a voltage input and output where the metric would be the open circuit voltage gain, $A_{v, oc}$, and the other for a current input and output with the metric being the short circuit current gain, $A_{i, sc}$ (commonly written $\beta_{sc}$):

![Diagram](image)

$$A_{v, oc}(s) = \frac{v_{out}(j\omega)}{v_{in}(j\omega)} = \frac{\frac{g_m - j\omega C_{gd}}{g_o - j\omega C_{gd}}}{g_m - j\omega C_{gd}}$$

$$\beta_{sc}(j\omega) = \frac{i_d(j\omega)}{i_g(j\omega)} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})}$$

Of these two alternatives, $\beta_{sc}$ is the more useful. $A_{v, oc}$ is derived with a voltage source driving a capacitor, something that doesn’t give a meaningful result and leads to ever increasing input power. It also does not involve $g_m$ and $C_{gs}$. Consequently, short circuit current gain is used as the intrinsic high frequency performance metric for transistors.
Intrinsic $\omega_{Hi}'s$ for MOSFETs - short-circuit current gain

The common-source short-circuit current gain is:

$$\beta_{sc}(j\omega) \equiv \frac{i_d(j\omega)}{i_g(j\omega)} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})}$$

there is one pole at $\omega = 0$, and one zero, $\omega_z$:

$$\omega_z = \frac{g_m}{C_{gd}}$$

The short circuit current gain, $\beta_{sc}$, is infinite at DC ($\omega = 0$), and its magnitude decreases linearly with increasing frequency.
Intrinsic $\omega_{HI}$'s for MOSFETs - short-circuit current gain, cont.

The magnitude of $\beta_{sc}$ decreases with $\omega$, but it is still greater than one for a wide range of frequencies.

$$|\beta_{sc}(j\omega)| = \frac{g_m^2 + \omega^2 C_{gd}^2}{\sqrt{\omega^2 (C_{gs} + C_{gd})^2}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called $\omega_t$. Setting $= 1$ and solving for $\omega_t$ yields:

$$\omega_t = \frac{g_m}{\sqrt{\left[\left(C_{gs} + C_{gd}\right)^2 - C_{gd}^2\right]}} \approx \frac{g_m}{C_{gs} + C_{gd}}$$
MOSFET short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Note: $\omega_z > \omega_t$

Low frequency value: infinity

Zero, $\omega_z$: $\omega_z = g_m/C_{gd}$

Unity gain point, $\omega_t$: $\omega_t @ g_m/(C_{gs} + C_{gd})$

No 3dB point, $\omega_b$. 
MOSFET short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Can we bias to maximize $\omega_t$?

$$\omega_t(MOSFET) = \frac{g_m}{(C_{gs} + C_{gd})} \approx \frac{g_m}{C_{gs}}$$

$$= \frac{W}{L} \mu_{Ch} C_{ox}^* |V_{GS} - V_T|$$

$$= \frac{2}{3} W L C_{ox}^*$$

$$= \frac{3}{2} \frac{\mu_{Ch} |V_{GS} - V_T|}{L^2}$$

Maximize $V_{GS}$.

What is the ultimate limit?

$$\omega_t(MOSFET) = \frac{3}{2} \frac{\mu_{Ch} |V_{GS} - V_T|}{L^2}$$

Lessons: Bias at well above $V_T$; make $L$ small, use n-channel.

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Lecture 24 - Slide 17
An aside: looking back at CMOS gate delays

CMOS: switching speed; minimum cycle time (from Lec. 15)

Gate delay/minimum cycle time:

For MOSFETs operating in strong inversion, no velocity saturation:

\[
\tau_{Min\, Cycle} = \frac{12nL_{min}^2 V_{DD}}{\mu_e \left[ V_{DD} - V_{Tn} \right]^2}
\]

Comparing this to the channel transit time:

\[
\tau_{Ch\, Transit} = \frac{L_{min}}{s_e Ch} = \frac{L_{min}}{\mu_e E_{Ch}} = \frac{L_{min}}{\mu_e \left( V_{DD} - V_{Tn} \right) / L_{min}}
\]

We see that the cycle time is a multiple of the transit time:

\[
\tau_{Min\, Cycle} = \frac{12nV_{DD}}{\left( V_{DD} - V_{Tn} \right)} \cdot \tau_{Channel\, Transit} = n' \tau_{Channel\, Transit}
\]

When velocity saturation dominated, we found the same thing:

\[
\tau_{Min\, Cycle} \propto \frac{L_{min} V_{DD}}{s_{sat} \left[ V_{DD} - V_{Tn} \right]} = n' \tau_{Chan\, Transit} \quad \text{where} \quad \tau_{Chan\, Transit} = \frac{L}{s_{sat}}
\]
Intrinsic $\omega_{Hi}$'s for MOSFETs - $\beta_{sc}(j\omega)$ and $\omega_t$ w. velocity saturation

What about the intrinsic $\omega_{Hi}$ of a MOSFET operating with full velocity saturation?

The basic result is unchanged; we still have:

$$\omega_t = \sqrt{\frac{g_m^2}{\left[(C_{gs} + C_{gd})^2 - C_{gd}^2\right]}} \approx \frac{g_m}{\left(C_{gs} + C_{gd}\right)} \approx \frac{g_m}{C_{gs}}$$

However, now $g_m$ is different:

$$g_m = W_s s_{sat} C_{ox}^*$$

With this we have:

$$\omega_t \approx \frac{g_m}{C_{gs}} = \frac{W s_{sat} C_{ox}^*}{W L C_{ox}^*} = \frac{s_{sat}}{L} = \frac{1}{\tau_{Ch}}$$

In the case where velocity saturation dominates, we once again find that it is the channel transit time that is the ultimate limit.

Do you care to speculate on the intrinsic $\omega_{Hi}$ of a BJT?
Intrinsic $\omega_{Hi}$'s for BJTs - short-circuit current gain

The common-emitter short-circuit current gain is:

$$\beta_{sc}(j\omega) = \frac{i_c(j\omega)}{i_b(j\omega)} = \frac{g_m - j\omega C_\mu}{g_\pi + j\omega(C_\pi + C_\mu)}$$

there is one pole, call it $\omega_p$, and one zero, $\omega_z$:

$$\omega_p = \frac{g_\pi}{(C_\pi + C_\mu)}, \quad \omega_z = \frac{g_m}{C_\mu}$$

Of these two, $\omega_p$ is much smaller and this is the 3dB point of the common-emitter short-circuit current gain. We give it the name $\omega_\beta$:

$$\omega_\beta = \frac{g_\pi}{(C_\pi + C_\mu)}$$
Intrinsic $\omega_{HI}$'s for BJTs - short-circuit current gain, cont.

The magnitude of $\beta_{sc}$ decreases above $\omega_b$, but it is still greater than one initially:

$$|\beta_{sc}(j\omega)| = \sqrt{\frac{g_m^2 + \omega^2C^2\mu}{g_\pi^2 + \omega^2(C_\pi + C\mu)^2}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called $\omega_t$. Setting $\omega = 1$ and solving for $\omega_t$ yields:

$$\omega_t = \frac{g_m}{\sqrt{\left[(C_\pi + C\mu)^2 - C\mu^2\right]}} \approx \frac{g_m}{(C_\pi + C\mu)}$$
BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Note: $\omega_z > \omega_t >> \omega_\beta$ (= $\omega_t/\beta_F$)

Low frequency value: $\beta_F$

Zero, $\omega_z$: $\omega_z = g_m/C_\mu$

3dB point, $\omega_b$: $\omega_b = g_m/(C_\pi+C_\mu)$

Unity gain point, $\omega_t$: $\omega_t @ g_m/(C_\pi+C_\mu)$
BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.

Can we bias to maximize $\omega_t$?

$$\omega_t \approx \frac{g_m}{(C_\pi + C_\mu)} = \frac{qI_C}{kT} + \left[\frac{qI_C}{kT}\tau_b + C_{eb,dp} + C_{cb,dp}\right]$$

**Maximize $I_C$.**

Used $C_\pi = g_m\tau_b + C_{eb,dp}$

In the limit of large $I_C$:

$$\lim_{I_C \to \infty} \omega_t \approx \frac{1}{\tau_b} = \frac{2D_{\text{min},B}}{W_B^2} = \frac{2\mu_{\text{min},B} V_{\text{thermal}}}{W_B^2}$$

**Lessons:** Bias at large $I_C$; make $w_B$ small, use npn.
Lecture 24 - Intrinsic Limits of Transistor Speed - Summary

• Intrinsic high frequency limits for transistors
  **General approach:** short-circuit current gains

• Limits for MOSFETs:
  **Metric - CS short-circuit current unity gain pt:** \( \omega_T = g_m / [(C_{gs} + C_{gd})^2 - C_{gd}^2]^{1/2} \)
  \( \omega_T \) is approximately \( g_m / C_{gs} = 3\mu_e (V_{GS}-V_T)/2L^2 \)
  \( g_m = (W/L)\mu_e C_ox^* (V_{GS}-V_T) \) and \( C_{gs} = (2/3)WLC_{ox}^* \)
  so \( \omega_T \approx 3\mu_e (V_{GS}-V_T)/2L^2 = 1/\tau_{ch} \)
  **Design lessons:** bias at large \( I_D \)
  minimize \( L \) (win as \( L^2 \); as \( L \) in velocity saturation)
  use n-channel rather than p-channel \( (\mu_e >> \mu_h) \)

• Limits for BJTs:
  **Metrics - CE short-circuit current gain 3B pt:** \( \omega_b = g_p / (C_{\pi} + C_{\mu}) \)
  **CE short-circuit current gain unit gain pt:** \( \omega_T = g_m / (C_{\pi} + C_{\mu}) \)
  \( \omega_T \) approaches \( 1/\tau_b \) as \( I_c \) increases and \( \tau_b = w_B^2 / 2D_{min,B} \)
  so \( \omega_T \approx 2D_{min,B} / w_B^2 = 2\mu_e V_t / w_B^2 = 1/\tau_b \)
  **CB short-circuit current gain unit gain pt:** \( \omega_\alpha = g_m / C_{\pi} \)
  **Design lessons:** bias at high collector current
  minimize \( w_B \) (win as \( w_B^2 \))
  use npn rather than pnp \( (\mu_e >> \mu_h) \)
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