Recitation 25: CMOS Cascade Amplifier

Last week, we talked about a particular example of multi-stage amplifier: CS-CB cascode amplifier. We used BJT/CMOS in the circuit (BICMOS).

Today we will look at the CMOS cascode amplifier with some specific requirement on $R_{\text{out}}$, and see how to generate $I_{\text{sup}}$ and $V_B$.

This is a CS-CG CMOS cascode amplifier. It has:

- $R_{\text{in}} \rightarrow \infty$
- $R_{\text{out}}$ very high (compare to CS only)
- Very good frequency response (close to CG, better than CS)
Example: Device Data

\[
V_{T_p} = -1 \text{V}, \quad \mu_p C_{\text{ox}} = 25 \mu \text{A/V}^2, \quad \lambda_p = 0.02 \text{V}^{-1} \\
V_{T_n} = 1 \text{V}, \quad \mu_n C_{\text{ox}} = 50 \mu \text{A/V}^2, \quad \lambda_n = 0.05 \text{V}^{-1}, \quad L = 2 \mu \text{m}
\]

Goal:

- design transconductance amplifier with \(G_m = 1 \text{mS}, \ R_{\text{out}} \geq 10 \text{MΩ}, \ R_{\text{in}} = \infty\).
- With 5 V power supply, 2 \(\mu\text{m}\) CMOS process.
- output drives other CMOS (capacitive load).
- Use \(I_{\text{sup}} = 100 \mu\text{A}\).

Small signal model of the circuit

\[
R_{\text{in}} = \infty \\
R_{\text{out}} = \gamma_{oc} || (\gamma_{o2} + \gamma_{o2} \cdot g_m R_s) = \gamma_{oc} || (\gamma_{o2} \cdot g_{m2} \cdot \gamma_{o1}) \\
R_s = \gamma_{o1}
\]

Overall \(G_m\) = \[
\frac{v_{\text{out}}}{v_s} = \frac{-i_{\text{in}2}}{v_s} = \frac{g_m v_{\text{gs}1} \left( \frac{\gamma_{o1}}{\gamma_{o1} + \gamma_{m2}} \right)}{v_s} = g_{m1}
\]

\[
\therefore G_m = g_{m1} = 1 \text{mS} \quad \Rightarrow \quad g_{m1} = \sqrt{2 \left( \frac{w}{L} \right) \mu_n C_{\text{ox}} I_D} = 1 \text{mS}
\]

Solve for \(w_1, \ w_1 = \frac{g_{m1}^2 \cdot L_1}{2 I_D \mu_n C_{\text{ox}}} = \frac{(1 \text{mS})^2 \cdot (2 \mu \text{m})}{2 \times 100 \mu \text{A} \cdot 50 \mu \text{A/V}^2} = 200 \mu \text{m}
\]

This is design on M1.
M2: output resistance requirement determines size of M2

\[ R_{\text{out}} \simeq \gamma_{oc} \left| g_{m2} \cdot \gamma_{o2} \cdot \gamma_{o1} \right| \geq 10 \text{ M\ensuremath{\Omega}} \]

Assume both \( \gamma_{oc}, g_{m2} \cdot \gamma_{o2} \cdot \gamma_{o1} \) are on the same order,

\[
\begin{align*}
\gamma_{oc} & \simeq g_{m2} \cdot \gamma_{o2} \cdot \gamma_{o1} \quad \Rightarrow \quad g_{m2} \cdot \gamma_{o1} \cdot \gamma_{o2} \geq 20 \text{ M\ensuremath{\Omega}} \\
\lambda_n & = 0.05 \text{ V}^{-1} \quad \Rightarrow \quad \gamma_{o1} = \gamma_{o2} = \frac{1}{\lambda_n I_D} = \frac{1}{(0.05 \text{ V}^{-1})(100 \mu\text{A})} = 200 \text{ k}\ensuremath{\Omega} \\
g_{m2} \cdot (200 \text{ k}\ensuremath{\Omega})(200 \text{ k}\ensuremath{\Omega}) & \geq 20 \text{ M\ensuremath{\Omega}} \quad \Rightarrow \quad g_{m2} \geq 5 \times 10^{-4} \text{ S} = 0.5 \text{ mS} \\
g_{m2} & = \sqrt{2I_D \left( \frac{w}{L} \right)_2 \mu_n C_{\text{ox}}} \quad \Rightarrow \quad \left( \frac{w}{L} \right)_2 = 25, \quad w_2 = 50 \mu\text{m}
\end{align*}
\]

**Current Source Design**

Now how to design current source \( I_{\text{sup}} \) so that \( \gamma_{oc} \geq 20 \text{ M\ensuremath{\Omega}} \)? Yesterday we talked about simple MOS current source

\[
I_{\text{out}} = \frac{(w/L)_{B3}}{(w/L)_{B}} I_{\text{REF}}
\]

\[
\Rightarrow \quad \text{need to cascode circuit for current source. Add a current buffer (CG) for high } R_{\text{out}}
\]

Source resistance of current supply

\[
R_{\text{out}} = \frac{1}{\lambda I_D} = \frac{1}{0.02 \text{ V} \times 100 \mu\text{A}} = 500 \text{ k}\ensuremath{\Omega}
\]
\[ R_{\text{current source}} = \frac{R_{\text{out of CG}}}{\gamma_o4 \cdot \gamma_o3} \cdot g_{m4} \cdot 500 \text{k} \Omega \cdot 500 \text{k} \Omega \geq 20 \text{M} \Omega \]

Need \( g_{m4} \), which is determined by size M4
Size of M3 and M4 is related to \( V_{G3} \) and \( V_{G4} \) to bias these gates, M3 and M4 need to be in saturation regime:

\[
V_{SD} > V_{SG} + V_{T_p} \quad \text{Choose} V_{SG} = 1.5 \text{V} \implies \text{minimum} V_{SD} = (1.5 - 1), V = 0.5 \text{V}
\]

(If we choose smaller \( V_{SG} \), we will need larger device \( \frac{w}{L} \) to carry 100 \( \mu \text{A} \))

\[
\begin{align*}
\text{with } & V_{SG} = 1.5 \text{V} \implies V_{G3} = 3.5 \text{V} \text{ and } V_{G4} = 2 \text{V} \\
\text{Since } & |I_{DP}| \sim w \frac{\mu_p C_{ox}(V_{SG} + V_{T_p})^2}{2L} = 100 \mu\text{A} \\
\left( \frac{1}{L} \right)_{3,4} & = \frac{2|I_{DP}|}{\mu_p C_{ox}(V_{SG} + V_{T_p})^2} = 32 = \frac{64}{2} \\
g_{m4} & = \frac{w}{L} \mu_p C_{ox}(V_{SG} + V_{T_p}) = 0.4 \text{mS}
\end{align*}
\]

(Size of M3B & M4B should be the same as for M4 and M3, helps in matching current flow). Then

\[
R_{\text{current source}} = g_{m4} \cdot \gamma_o4 \cdot \gamma_o3 = (0.4 \text{ mS})(500 \text{k} \Omega)(500 \text{k} \Omega) \]
\[
= 100 \text{ M} \Omega > 20 \text{ M} \Omega
\]
What does the design look like so far?

⇒ Need voltage source for $V_B$. Use diode connected NMOS (M2B) between $I_{REF}$ and PMOS
Make M2B same size as M2, \((\frac{w}{L})_{2B} = 50/2\) and:

\[
V_{GS_2} = V_{GS_{2B}} = V_{T_n} + \sqrt{\frac{2I_{REF}}{(\frac{w}{L})_2 \mu_n C_{ox}}} = 1.4 \text{ V}
\]
Output Voltage Swing

upswing: M4 must stay in saturation regime
\[ V_{SD_4} \geq V_{SG_4} + V_T \implies V_{SD_4} \geq 1.5\,V - 1\,V = 0.5\,V \]
Since \( V_{S_4} = 3.5\,V \implies V_{D_4} \leq 3\,V \)

down swing: M2 must stay in saturation regime
\[ V_{DS_2} \geq V_{GS_2} - V_{T_n}, \quad V_{DS_2} \geq 1.4\,V - 1.0\,V = 0.4\,V \]
Since \( V_{S_2} = 0.6\,V, \quad V_{D_2} \geq 1\,V \]
\[ \implies \quad \text{Swing is } 1.0\,V \leq V_{out} \leq 3.0\,V \]