6.111 Lecture # 18

More Video

MC6847 Display Controller
Obsolete but useful
All Points Addressable
Digital System Side
MC6847 with Character ROM

Note the hardware hack
To get around a bug in way /HS is generated
(The first /HS of a frame is AFTER the first row of dots)
Black and White (or Green)

Simple way of driving monitor
Has composite sync on the video
Adjust pot (top) so bottom of sync pulse has V=0
Color Output

Need to decode the 'chroma' outputs
Comparators on left decode
Gates on right drive RGB

AM25LS32 has fast comparators
'S38 is open collector NANDs
Vertical Sync Generation

MC6847 generates blanking but not the vertical sync pulse
Here is one legitimate use for one-shots

![Diagram of vertical sync generation](image)

**RGB Cable**
Pin 1  Intensity  
Pin 2  Reg  
Pin 3  Green  
Pin 4  Blue  
Pin 5  GND  
Pin 6  GND  
Pin 7  HSYNC  
Pin 8  VSYNC
LM1882 Sync Generator

Programmable, flexible part
Sync Generator: Setup

Store timing information in registers

Example
256 pixels wide
256 lines
5 MHz clock (probably not typical)
Sync Generator: Register Contents

Register Contents:

Horizontal (Line) Control

R1  8  Horizontal Front Porch
R2  32 Horizontal Sync Pulse End
R3  56 Horizontal Blanking
R4  312 Line Width

Time in "clocks"

Vertical (Frame) Control

R5  4  Vertical Front Porch
R6  7  Vertical Sync Pulse End
R7  21 Vertical Blanking
R8  276 Frame: 256 lines + 20 lines blanking

Lines

Register 0: Contents 011000011000

Bit 10: Enable System Clock
Bit 9: Disable Equalization
Bits 8:5 Sync Pulses Active Low
Bits 4:3 Non-Interlaced
Bits 2:0 Default Output Config:

Pin 12 CBLANK. Pin 13 HGATE. Pin 14 CSYNC. Pin 15 VGATE
Sync Generator: Physical Setup

LM1882 must be loaded on power up
Use a ROM (PROM) to hold configuration
Your MCU or FSM must do the programming
Sync Generator: Timing of Config

This is "Manual Addressing" mode
See data sheet for more

Manual Addressing Mode

<table>
<thead>
<tr>
<th>Cycle #</th>
<th>Load Falling Edge</th>
<th>Load Rising Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enable Manual Addressing</td>
<td>Load Address m</td>
</tr>
<tr>
<td>2</td>
<td>Enable Lbyte Data Load</td>
<td>Load Lbyte m</td>
</tr>
<tr>
<td>3</td>
<td>Enable Hbyte Data Load</td>
<td>Load Hbyte m</td>
</tr>
<tr>
<td>4</td>
<td>Enable Manual Addressing</td>
<td>Load Address n</td>
</tr>
<tr>
<td>5</td>
<td>Enable Lbyte Data Load</td>
<td>Load Lbyte n</td>
</tr>
<tr>
<td>6</td>
<td>Enable Hbyte Data Load</td>
<td>Load Hbyte n</td>
</tr>
</tbody>
</table>
Sync Separator

Reverse Direction
Generate Composite Sync from Video
Generate separated sync signals too

From Camera → GS4981
→ Composite Sync
→ Vertical Sync
→ Horizontal Sync
→ Back Porch
Getting Information Here to There

Full Handshake: Timing
No info gets lost

Parallel Interface, Full Handshake
Serial Interface

RS-232 is a serial interface standard
What is shown here is TTL signal
RS-232 levels are inverted from this
UART

Universal Asynchronous Receiver/Transmitter
Increasingly less common devices
Example is the AY-3-1015D (now obsolete but useful)
AY-3-1015D Transmit Section
Transmission Lines

Signals travel on wires
Attenuation -- losses
Reflections -- affected by terminations

Transmission Line has characteristic parameters:

- $L$: Inductance per unit length
- $C$: Capacitance per unit length
- $Z_0$: Characteristic Impedance
- $U_0$: Phase Velocity

\[
Z_0 = \sqrt{\frac{L}{C}}
\]

\[
U_0 = \sqrt{\frac{1}{LC}}
\]
Signal Propagation

Pulses traveling on the line
Voltage and Current
Ratio of voltage to current is 'characteristic impedance'
Sign of that ratio is direction of propagation
Propagate at $< C$ (speed of light)

\[ V_+ = Z_0 I_+ \]
\[ V_- = -Z_0 I_- \]
Pulses are absorbed if receiving end is matched
If not matched, pulse 'reflects'
Sign of reflected wave depends on impedance:
Characteristic Impedance Demo

Reflections depend on terminating impedance
Can be minimized by terminating correctly
**Crosstalk Demo**

**Flat Ribbon Cable**
- Similar to kit interconnect cables
- Wires situated next to each other
- Capacitive and inductive coupling

**Crosstalk minimized by alternating wires**
- Ground - Signal - Ground - Signal ...

![Diagram of flat ribbon cable showing alternating ground and signal wires.](image)