Homework #1 : Solutions

1. [Plummer 1.4] Estimate the resistivity of pure Si in Ω-cm at (a) room temperature (b) 77°K (c) 1000°C
Neglect the temperature dependence of carrier mobilities.

From Plummer, Eq. 1.1, we have:

\[ \rho = \frac{1}{\mu n + \mu p} \]

where

\[ q = 1.6 \times 10^{-19} \text{C} \]

\[ m_n = 1500 \text{ cm}^2/\text{V.s} \]

\[ m_p = 500 \text{ cm}^2/\text{V.s} \]

Since we are assuming that the mobility of electrons, \( m_n \),
and the mobility of holes, \( m_p \), is independent of
temperature, we need to determine the concentration of
electrons and holes, \( n \) and \( p \) respectively, at the
given temperature.

In pure (undoped) silicon, \( n = p \) due to charge neutrality.
A hole and an electron are generated simultaneously
when an electron breaks free from the outer orbital of
a silicon atom. Keep in mind that this is not the
case for doped silicon. In n-type silicon \( n > p \)
and vice versa in p-type silicon.

From the law of mass action (Plummer Eq. 1.3), we
have \( n p = n_i^2 \) where \( n_i \) is dependent on temperature
and can be approximated by Plummer Eq. 1.4:

\[ n_i = 3.1 \times 10^{16} T^{3/2} \exp \left( \frac{-0.603 \text{eV}}{k_b T} \right) \text{[cm}^3\text{]} \] (for silicon)

Since \( n = p \) for undoped Si, \( n = p = n_i \)

Note that \( T \) has units of Kelvin and \( k_b = 1.38 \times 10^{-23} \text{J/K} \)
\[ -02 - k_b = 8.625 \times 10^{-5} \text{eV/K} \]
(a) From the text, we are given that $n_i = 1.45 \times 10^{10} \text{cm}^{-3}$ for silicon at room temperature. We can use this value in Eq. 1.1 and solve the problem but let us use the value we obtain with Eq. 1.4.

$$n_i = 3.1 \times 10^{16} \left( \frac{(300)^{3/2} \exp \left( \frac{-0.603}{8625} \right)}{8625/65000} \right) = 1.22 \times 10^{10} \text{cm}^{-3}$$

This value is on the same order as the value given in the text. The difference is due to round off error.

$$\therefore \rho = \left[ 1.6 \times 10^{-19} \left( 1500 \text{cm}^3/\text{V.s} + 500 \text{cm}^3/\text{V.s} \right) (1.22 \times 10^{10} \text{cm}^{-3}) \right]^{-1}$$

$$\rho = 2.56 \text{ k}\Omega \cdot \text{cm}$$

(b) @ 373°K, $n_i = 7.74 \times 10^{-21} \text{cm}^{-3} \approx 0$

We clearly see evidence of freeze out. There is a very small amount of carriers that are thermally generated.

$$\therefore \rho = 4.04 \times 10^{35} \Omega \cdot \text{cm} \approx \text{near infinite}$$

⇒ essentially a perfect insulator

(c) @ 1000°C = 1273°K, $n_i = 5.80 \times 10^{18} \text{cm}^{-3}$

$$\therefore \rho = 5.39 \times 10^{-4} \Omega \cdot \text{cm}$$

Comparing this value to the resistivity of Aluminum at room temperature ($2.8 \times 10^{-6} \Omega \cdot \text{cm}$), we can see that the silicon is essentially metallic.

* In the more recent printing of Plummer, Equation 1.4 is actually: (corrected error)

$$n_i = 3.9 \times 10^{16} T^{3/2} \exp \left( \frac{-0.603 \text{eV}}{kT} \right) \text{cm}^3$$
(2) [Plummer 1.10] - A state of the art NMOS might have a
drain junction area of 0.5 x 0.5 \text{mm}^2. Calculate junction
capacitance at applied reverse bias of 2V assuming
drain is heavily doped and substrate doping is 1\times10^{18}\text{cm}^{-2}.

**Standard NMOS** - Configuration where bulk and source are tied to the
same potential.

Focus on the PN Junction formed by the drain and
bulk

&gt; If the junction is reverse biased, and
we assume that the bulk is at ground,
then the voltage at the drain is +2V.

From the text, we have the following equations for
a PN-junction:

\[
C_p = \frac{k_BT}{q} \ln \left( \frac{N_{D,N}}{N_{C,N}} \right) \quad \text{[Plummer Eq. 1.24]}
\]

\[
\frac{C}{A} = \frac{\epsilon_s}{\epsilon_d} = \left[ \sqrt{\frac{4\epsilon_s}{2} \left( \frac{N_{A,N}}{N_{A,N}} \right)(V+2V)} \right] \quad \text{[Plummer Eq. 1.25]}
\]

Assuming that the drain is heavily doped, \( N^+ \) or \( N^{++} \)

\( N^+ : 10^{18}\text{cm}^2 < n < 10^{20}\text{cm}^3 \) ; \( N^{++} : 10^{20}\text{cm}^3 < n \)

Note that assuming \( N^{++} \), n cannot exceed \( 10^{22}\text{cm}^3 \) since
the semiconductor becomes degenerate and the equation
for \( C_i \) would not be entirely accurate.
if we want to find the junction capacitance, we use Plummer Eq. 125:

\[ C = A \sqrt{\frac{q \varepsilon_s}{2} \left( \frac{N_{A+} \varepsilon_s}{N_{A+} + N_D} \right) \left( \frac{1}{Q_i + V} \right)} \approx A \sqrt{\frac{q \varepsilon_s}{2} \left( \frac{N_A}{Q_i + V} \right)} \]

(positive sign since reverse biased - increases the depletion width, lowering the capacitance)

⇒ the approximation above is valid since \( N_D \gg N_A \)

* The region with lighter doping has more control on the junction capacitance.

Assuming room temperature, \( N_L = 1.45 \times 10^{16} \text{ cm}^{-3} \), and knowing that \( p^n N_A = 1 \times 10^{16} \text{ cm}^{-3} \), we can solve for \( Q_i \) for assumed concentrations of \( N_D \).

\[ \frac{kT}{q} \approx 26 \text{ mV} \text{ at room temperature} \quad \text{(good value to memorize)} \]

so \( Q_i = \begin{cases} 
\approx 0.82 \text{ V} & \text{at } 1 \times 10^{18} \text{ cm}^{-3} \\
\approx 0.88 \text{ V} & \text{at } 1 \times 10^{19} \text{ cm}^{-3} \\
\approx 0.94 \text{ V} & \text{at } 1 \times 10^{20} \text{ cm}^{-3} 
\end{cases} \]

or assume 0.94 V

For the following work, I am assuming \( N_D = 1 \times 10^{20} \text{ cm}^{-3} \Rightarrow Q_i = 0.94 \text{ V} \)

\( \varepsilon_s = 11.7 \Rightarrow 11.7 \left( 8.85 \times 10^{-12} \text{ F/m} \right) = 1.035 \times 10^{-12} \text{ F/cm} \)

\[ C = \left[ 0.5 \times 10^{-4} \text{ cm} \right]^2 \sqrt{\frac{2 \varepsilon_s}{2} \left( 1 \times 10^{16} \text{ cm}^{-3} \right) \frac{1}{(0.94+2)}} = 4.12 \times 10^{-12} \text{ F} \]

(b) compare to gate capacitance of the same area with \( SiO_2 \) thickness of 2.5 nm. Assume silicon is a metal

\[ \varepsilon_0 = 3.9 \varepsilon_0 \Rightarrow 3.9 \times 8.85 \times 10^{-12} \text{ F/m} = 3.4515 \times 10^{-11} \text{ F/m} \]

\[ C = \frac{\varepsilon_0 x A}{d_{ox}} = \frac{3.4515 \times 10^{-11} \text{ F/m} \left( 0.5 \times 10^{-6} \text{ m} \right)^2}{2.5 \times 10^{-9} \text{ m}} = 3.45 \times 10^{-15} \text{ F} \]

4.
Cross section is a simple bipolar transistor design. a feasible process flow you don't have to include any quantitative process parameter. Annu should be selected, explaining for each step and order chosen.

- Silicon
- Silicon Dioxide
- Metallization
- Photoreist

There are many correct answers to this problem. The point of this exercise is to make you think about a process flow and to keep track of process history.

1. Start with p-type wafer, grow thin oxide by dry oxidation (to prevent channeling), coat and pattern resist, then implant phosphorus ions to form N+ region that is "buried".
2. Strip resist with O2 plasma or chemical wet etch, strip oxide with plasma or buffered oxide etch (dilute HF), anneal to repair lattice from implant, grow in situ n-type epitaxial layer.
3. Grow thin oxide with thermal oxidation, coat and pattern resist, then implant boron ions to form p+ well and p+ isolation regions.
- Dry or wet etch oxide using previous resist as mask.
  Strip the resist with O$_2$ plasma.
  Perform a chemical etch, coat and pattern a new layer of resist.
  Implant more boron ions to complete p$^+$ isolation regions.
  Note that there is no oxide, permitting ions to travel deep into the epitaxial layer.

- Strip resist, anneal, digest oxide using chemical vapor deposition (CVD), coat and pattern resist.
  Use dry or wet etch to pattern the oxide for the N$^+$ implants and contacts.

- Strip resist, grow thin layer of thermal oxide. Coat and pattern new resist layer for phosphorus ion implant to form N$^+$ regions. The thermal oxide is to keep the implants shallow.

- Strip old resist, anneal, coat and pattern new resist for oxide etch to form contacts to the base, emitter, and collector of the BJT.
  Etch the oxide to expose contact regions.

To obtain the final cross section, strip the resist, spin and pattern new resist for metallization (sputter metal, shield new resist, and anneal the wafer so metal forms a denser film.)