Problem 1: Device Parameters

The data from five measurements made on a short channel NMOS device appears in Table 1. Given that 
\( V_{DSAT} = 0.6\, V \) and \( k' = 100\, \mu A/V^2 \), calculate \( V_{TH}, \gamma, \lambda, 2|\phi_F|, \) and \( W/L \).

<table>
<thead>
<tr>
<th>Meas. Number</th>
<th>( V_{GS} )</th>
<th>( V_{DS} )</th>
<th>( V_{BS} )</th>
<th>( I_D (\mu A) )</th>
</tr>
</thead>
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<tr>
<td>1</td>
<td>2.5</td>
<td>1.8</td>
<td>0</td>
<td>1812</td>
</tr>
<tr>
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<td>2</td>
<td>1.8</td>
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<td>1297</td>
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<td>2</td>
<td>1.8</td>
<td>-1</td>
<td>1146</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>1.8</td>
<td>-2</td>
<td>1039</td>
</tr>
</tbody>
</table>

Problem 2: Backgate Effect

The circuit in Fig. 1 is known as the source follower configuration. It achieves a DC level shift between the 
input and the output. The value of this shift is determined by the current \( I_0 \). Assume \( \gamma_d = 0, \gamma = 0.4, 2|\phi_F| = 0.6\, V, \) 
\( V_{TH} = 0.43\, V, k_n' = 115\, \mu A/V^2 \) and \( \lambda = 0 \).

![Figure 1: NMOS source follower configuration](image-url)
a) Suppose we want the nominal level shift between \( V_i \) and \( V_o \) to be 0.6V in the circuit in Figure 1(a). Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate \( V_i \) to \( V_o \) in terms of \( I_o \)).

b) Now assume that an ideal current source replaces M2 (Figure 1(b)). The NMOS transistor M1 experiences a shift in \( V_T \) due to the backgate effect. Find \( V_T \) as a function of \( V_o \) for \( V_o \) ranging from 0 to 2.5V with 0.5V intervals. Plot \( V_T \) vs. \( V_o \).

c) Plot \( V_o \) vs. \( V_i \) as \( V_o \) varies from 0 to 2.5V with 0.5V intervals. Plot two curves: one neglecting the backgate effect and one accounting for it. How does the backgate effect influence the operation of the level converter?

At \( V_o \)(with backgate effect) = 2.5V, find \( V_o \)(ideal) and thus determine the maximum error introduced by the backgate effect.

**Problem 3: Velocity Saturation**

This problem explores the behavior of short-channel devices. For the HSPICE simulations of this problem you will use the 0.18u model parameters. Use the HSPICE model parameters which can be found in “log018_1.l”

a) Using HSPICE plot \( I_D \) versus \( V_{DS} \), for the transistor of the following figure, with \( V_{GS} \) (0.6V, 0.8V, 1V, 1.2V, 1.4V, 1.6V, 1.8V) as a parameter. Comment on the dependence of \( I_D \) with respect to \( V_{GS} \).

b) Calculate the effective resistance for a high to low transition, using the method described in slide 44 (Handout 2).

c) Consider two CMOS inverters with \( (W_1/L_1)_n = (2.88u/1.44u) \) and \( (W_1/L_1)_p = (5.76u/1.44u) \) and \( (W_2/L_2)_n = (0.36u/0.18u) \) and \( (W_2/L_2)_p = (0.72u/0.18u) \). Assume \( V_{DD} = 1.8 \) V and the output of the inverter is loaded by \( C_L = 100\text{fF} \) capacitance. Calculate the propagation delay \( t_p \) and check the answers with HSPICE.

d) Repeat part c) sweeping the supply voltage \( V_{DD} \) from 0.4V to 1.8V (sweep step 0.2V). Plot the propagation delay \( t_p \) versus the supply voltage \( V_{DD} \) in the same graph. Comment on the results.

**Problem 4: Voltage transfer characteristics, Noise Margins**

The next figure shows an all NMOS inverter.
a) Calculate $V_{OH}$, $V_{OL}$, and $V_M$ for the new inverter.

\[ V_{DD} = 2.5V \]

\[ M_2 \text{ W/L=0.375/0.25} \]

\[ M_1 \text{ W/L=0.75/0.25} \]

**Figure 3:** An Alternate Inverter Implementation

b) Use HSPICE to obtain the VTC.

c) Calculate $V_{IH}$, $V_{IL}$, and the noise margins and comment on the results. How can you increase the noise margins and reduce the undefined region?

d) Comment on the differences in the VTCs, robustness and regeneration between this inverter and a standard CMOS inverter.

**Problem 5: Inverter Gain and Regions of Operation**

The Figure 4 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at $V_M$. The intersection of this line with the $V_{OH}$ and the $V_{OL}$ lines defines $V_{IH}$ and $V_{IL}$.

\[ V_{out} \]

\[ V_{OH} \]

\[ V_M \]

\[ V_{OL} \]

**Figure 4:** A Different Approach to Derive $V_{IL}$ and $V_{IH}$
a) The noise margins of a CMOS inverter are highly dependent on the sizing ratio, \( r = \frac{k_p}{k_n} \), of the NMOS and PMOS transistors. Use HSPICE with \( V_{Tn} = |V_{Tp}| \) to determine the value of \( r \) that results in equal noise margins? Give a qualitative explanation.

b) Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for \( NM_H \) and \( NM_L \) in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at \( V_M \). For what range of \( r \) is this assumption valid? What is the resulting range of \( V_M \)?

c) Use the method from section 5.3.2 to derive an expression for the inverter gain at \( V_M \) for the case when the sizing ratio is chosen to place \( V_M \) just below limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS?

### Problem 6: Static CMOS Inverter

For this problem use scalable CMOS design rules and assume:

\[
V_{DD} = 2.5V, \quad \frac{W_p}{L} = 1.25/0.25, \quad \frac{W_n}{L} = 0.375/0.25, \quad L = L_{eff} = 0.25\mu m \quad (i.e. \quad x_d = 0\mu m), \quad C_L = C_{inv-gate}, \quad k_p' = 115 \mu A/V^2, \quad k_n' = -30 \mu A/V^2, \quad V_{tn0} = V_{tp0} = 0.4V, \quad \lambda = 0V^{-1}, \quad \gamma = 0.4, \quad 2|\phi_p| = 0.6V, \quad \text{and} \quad \tau_{ox} = 58A. \]

Use the Hspice model parameters for parasitic capacitance given below (i.e. \( C_{gd0}, C_{j}, C_{jsw} \)), and assume that \( V_{SB} = 0V \) for all problems except part (e).

**Figure 5:** CMOS inverter with capacitive load.

```plaintext
## Parasitic Capacitance Parameters (F/m)##
NMOS
CGDO=3.11x10^{-10}, CGSO=3.11x10^{-10}, CJ=2.02x10^{-3}, CJSW=2.75x10^{-10}

PMOS
CGDO=2.68x10^{-10}, CGSO=2.68x10^{-10}, CJ=1.93x10^{-3}, CJSW=2.23x10^{-10}
```

a) What is the \( V_m \) for this inverter?

b) What is the effective load capacitance \( C_{Leff} \) of this inverter? (include parasitic capacitance, refer to notes for \( K_{eq} \) and \( m \).) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, \( \lambda = 0.125 \mu m \), and the source/drain extensions are \( 5\lambda \) for the PMOS; for the NMOS the source/drain contact regions are \( 5\lambda \times 5\lambda \).
c) Calculate \( t_{PHL}, t_{PLH} \) assuming the result of (b) is \( 'C_{Eff} = 6.5fF' \). (Assume ideal step input, i.e. \( t_{rise}=t_{fall}=0 \). Do this part by computing the average current used to charge/discharge \( C_{Eff} \).)

d) Find \( (W_p/W_n) \) such that \( t_{PHL} = t_{PLH} \).

e) Suppose we increase the width of the transistors to reduce the \( t_{PHL}, t_{PLH} \). Do we get a proportional decrease in the delay times? Justify your answer.

f) Suppose \( V_{SB} = 1V \), what is the value of \( V_{tn}, V_{tp}, V_m \)? How does this qualitatively affect \( C_{Eff} \)?

g) Use Magic to create a layout for this inverter. Extract the schematic, including parasitic capacitance, from the layout and use HSPICE to simulate the circuit and measure \( t_p \) and the average power for the following input \( V_{in} \): pulse(0 \( V_{DD} \) 5n 0.1n 0.1n 9n 20n), as \( V_{DD} \) varies from 1V - 2.5V with 0.25V interval. \( t_p = (t_{PHL} + t_{PLH}) / 2 \). Using this data, plot ‘\( t_p \) vs. \( V_{DD} \)’, and ‘Power vs. \( V_{DD} \)’.

The extracted layout will include parasitics so you need not manually include AS, AD, PS, PD in your spice deck, but remember to manually add \( C_L = 6.5fF \). Set \( V_{SB} = 0V \) for this problem. Use the HSPICE model parameters which can be found in “logic025.l”.

h) Using HSPICE, simulate the circuit for a set of ‘pulse’ inputs with rise and fall times of \( t_{in,rise,fall} = 1ns, 2ns, 5ns, 10ns, 20ns \). For each input, measure (1) the rise and fall times \( t_{out,rise} \) and \( t_{out,fall} \) of the inverter output, (2) the total energy lost \( E_{total} \) and (3) the energy lost due to short circuit current \( E_{short} \). For measuring short circuit power, use the technique discussed in class (slide 96, Handout 2). Use the HSPICE model parameters which can be found in “logic025.l”.

Using this data, prepare a plot of (1) \( (t_{out,rise}+t_{out,fall})/2 \) vs. \( t_{in,rise,fall} \), (2) \( E_{total} \) vs. \( t_{in,rise,fall} \), (3) \( E_{short} \) vs. \( t_{in,rise,fall} \) and (4) \( E_{short}/E_{total} \) vs. \( t_{in,rise,fall} \).

Provide simple explanations for:
(i) Why the slope for (1) is less than 1?
(ii) Why \( E_{short} \) increases with \( t_{in,rise,fall} \)?
(iii) Why \( E_{total} \) increases with \( t_{in,rise,fall} \)?