Lecture 25 - Optoelectronic Integrated Circuits - Outline

• Motivation: proposed OEIC applications
  Inter- and intra-chip optical interconnect and clock distribution
  Fiber transceivers
  Intelligent sensors
  Smart pixel array parallel processors

• Challenges
  Materials mismatches: lattice period; thermal expansion
  Wafer incompatibilities: diameter mismatch

• Approaches
  Conventional hybrid assembly: multi-chip modules
  Total monolithic process development
  Modular integration on ICs:
    epitaxy-on-electronics
    flip-chip bump bonding w. substrate removal
    self-assembly (extreme hybrid or pseudo-monolithic?)
Optical Solder Bumps: IC chip mounted multi-chip module substrate

- Metal solder bumps
- Optical solder bumps sources detectors
- Optical signals on-chip interconnection

Silicon IC Chip (inverted)

Optical signals chip-to-chip interconnects

Conventional metal interconnect lines for power, ground, and electrical signal distribution

Planar optical waveguides for optical signal distribution

Multichip Module Substrate
OEIC Applications: Smart Pixel Arrays
“computation, parallel processing of data and images, en/decryption”

Information transfers -
In-plane: electrical
Plane-to-plane: optical

Smart pixel arrays
Diffractive element arrays

Light beams

Concept:
The plane-to-plane coupling pattern can be dynamically reconfigured by selecting which VCSELs are illuminated.
OEIC Applications: Diffuse optical tomography
“seeing beneath the skin: tumors, blood vessels, bones, etc.”

INDOCHIP:
An OEIC chip with interwoven arrays of detectors and emitters.

USE:
Procedure:
Each VCSEL is illuminated in turn and the pattern of scattered light seen by the detector array is recorded. With this information an image of the sub-surface structure can be constructed.

Note: Near infrared light is strongly scattered but only weakly absorbed in soft body tissue.
Understanding the Significance of the Difference in the Thermal Expansion Coefficients of Si and GaAs

Wafers of Si and GaAs with identical diameters of 150 mm* (6 in) at 15°C:

If the temperature is raised 100°C.....
....the GaAs wafer becomes 70µm larger than the Si wafer!

- If the wafers are bonded, the stress is destructively large (i.e. they break)
- If the wafers are not bonded, any patterns on them are badly misaligned.

- and -

A change of 100°C is small; 500°C or greater is more typical.

* The industrial norm for Si is 200 mm (8 in), with 300 mm (12 in) diameter wafers becoming more common.
The other mismatch: Wafer Diameter Mismatch

The newest silicon processes are fabricated on 200 mm (8 in), and more likely 300 mm (12 in), diameter wafers:

- Silicon $d = 300$ mm
- Silicon $d = 200$ mm
- GaAs $d = 150$ mm
- InP $d = 100$ mm

The largest GaAs wafers in production are 150 mm (6 in) diameter and the largest InP wafers are 100 mm (4 in) diameter.

This diameter mismatch must be dealt with just as the thermal expansion mismatch must be dealt with!
Optoelectronic integration - solder ball flip-chip assembly on opto-multi-chip module

- Flip-chip p-i-n diode astride polymer waveguide/mirror

Waveguide cross-section: 10 by 10 µm
Die size: 750 µm square by 250 µm thick
**Optoelectronic integration** - solder ball flip-chip assembly on a silicon chip

- Lasers or detectors flip-chip mounted on silicon chips with v-grooves etched to align to optical fibers (concept drawings)

Note: V-grooves are formed using anisotropic etchants that reveal <111> planes

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**Perspective**

Before:

**After:**

End view

The pulling and wetting action of the molten solder is strong enough to align the chips to the under-lying electronics.

C. G. Fonstad, 5/03
OEIC Processes - Indium bump bonding with substrate removal

(Images deleted)

• **BAE Systems, Xanoptics:**
  Above: Schematic of process sequence
  Right: Solder bump formation and alignment
  Lower left: Photomicrograph of solder bump array.
  Lower right: Cross-section of QWIP array integrated using indium solder bump bonding
OEIC Processes  - Bump bonding with substrate removal

(U. of Colorado co-planar process)
Left: Full assembly process
Above: Top view of IC before and after integration
Below: VCSEL prior to bonding (left) and after integration (rt)

OEIC Processes - Bump bonding with substrate removal, cont.

U. of Colorado top-bottom process
Left: Full assembly process
Below: Top view of IC after integration

OEIC Processes - Bump bonding with substrate removal, cont.

U. of Colorado top contact process
Left: Full assembly process
Below: Top view of IC after integration

(Images deleted)
OEIC Processes - Bump bonding with dual-use heterostructures and substrate microlenses

- UCSB
  Right: Cross-section of full assembly
  Lower left: VCSELs and detectors fabricated from the same heterostructure
  Lower right: Microlens array on substrate

OEIC Processes - Total monolithic process development

- 4 full monolithic examples:
  - pin-HBT:
  - msm-HFET:
  - pin-HFET:
  - WGPD-HFET:
The Optical Solder Bump Concept for Integrating GaAs- and InP-based Heterostructure Devices with Si-CMOS ICs

Prof. Clifton G. Fonstad, MIT

**Importance:** A powerful, monolithic approach to doing mixed-material, mixed-function integration

**Features:** Commercial foundry ICs and heterostructures
- Modular and monolithic; wafer-scale, batch processing
- Planar topology; compatible with solder bump packaging

**Current effort:** Integrate and characterize high-speed 1550 nm photodiodes on CMOS chips; evaluate optical clock distribution concepts.

**Future work:** Develop the ultimate optical solder bump technology,
Magnetically Assisted Statistical Assembly (MASA). MASA will enable us to integrate anything with anything!
The MIT Approach to Monolithic Optoelectronic Integration

Commercially processed, custom-designed IC wafer with recesses for adding photonic devices

Photonic device heterostructures located in their recesses

Heterostructures processed into photonic devices interconnected with pre-existing electronics

The power is in the concept.
The challenge is in filling the recesses....

Output

VCSEL
Epitaxy-on-Electronics (EoE)

- Commercially processed GaAs electronics (circuitry custom-designed using standard layout and simulation tools; chips obtained through MOSIS)
- Monolithic processing, high surface planarity, no excessive overcoating of optoelectronic devices
- All processing compatible with full-wafer and batch processing (no lattice or thermal expansion coefficient mismatch)
- Conventional growth and fabrication of optoelectronic devices (growth temperatures must be under 475°C)
An EoE-integrated LED on OPTOCHIP

FIBE Cross-section by Dr. K. Edinger and Prof. J. Melngailis, Laboratory for Ion Beam Research and Application, University of Maryland

LED in dielectric growth well
Light shield
InGaAsP LED
n+ GaAs buffer
n+ S/D implant
Semi-insulating GaAs substrate
Top-side contact
Back-side contact

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Courtesy of Dr. Edinger and Prof. Melngailis. Used with permission.
Photo by Prof. Melngailis, melng@eng.umd.edu. Specimen provided by Prof. Fonstad.
**Aligned Pillar Bonding (APB)**

- Optoelectronic heterostructures can be grown under optimal conditions on optimum substrates; bonded to GaAs or SOS
- All features of EoE process retained; 3-d and SOS options added
- Near-room temperature bonding would enable integration of InP-based optoelectronics and silicon-based electronics
Layout of MIT MARCO Interconnect Focus Center CMOS optical clock distribution test chip
- designed and laid out by Nigel Drego and Mike Mills (Prof. D. Boning)

Comments
Technology: 0.18 µm CMOS
Chip size: 2.2 x 2.2 mm
Key feature: Designed to add photodetectors by aligned pillar bonding (APB)
Recesses: 17
p-i-n detectors: InGaAs/InP (MBE-grown by Prof. Yoon Soon Fatt at NTU in Singapore)
Dielectric recess on CMOS chip
-recess geometry on MIT MARCO IFC optical clock distribution test chip
- PiN heterostructures grown by Prof. Yoon Soon Fatt, NTU, Singapore -

Comments
Recess size: 50 by 50 microns
Pillar size: 40 by 40 microns
Recess bottom/back contact: formed in metal 2
Upper pad/top contact: formed in metal 7
Optical clock distribution using picosecond pulses

The challenge: The capacitance on Node A must be 10 fF, or less.

Single heterostructure implementation
- one of the bonding pads must be connected to Node A, which adds significant parasitic capacitance.

Two heterostructure implementation
- Using two heterostructures, Node A can be made to add negligible parasitic capacitance.

RM³ integration makes it possible to meet the sub-10 fF challenge!
Concepts for applying RM$^3$ Integration
(Recess mounting with monolithic metallization)

to intra- and inter-chip optical interconnect

RM$^3$-integrated multi-contact laser diodes

Optical waveguide "metal" layer

On-chip interconnect using in-plane lasers and detectors coupled via planar optical waveguides formed in a dielectric interconnect “metal” layer

RM$^3$-integrated SiGe and InP mini-ICs

Chip-to-chip interconnect at 40 Gbps using SiGe or InP mini-IC mux’s/demux’s, multi-contact in-plane lasers and detectors, and flexible planar waveguide ribbon cables
Nano-pill assembly on processed Si IC wafes

Device pills patterned through epilayers. Device pills etched free of substrate.

Dielectric device recesses etched into CMOS wafer.

Device pills tumbled over recesses on CMOS wafer.

Device pills in place filling all recesses on CMOS wafer.
III-V Heterostructure Nanopills
- a GaAs nanopill etched free of its substrate

Dimensions: diameter = 45 µm; height = 5 µm
OEIC Processes - DNA-assisted self assembly

• Two implementations:

Right: DNA-assisted attachment to a carrier substrate, with subsequent transfer and bonding to final Si host.

Below: DNA-assisted attachment to host Si substrate directly

(Images deleted)


• Lock-and-key DNA-like chemicals are used to encourage nanopills to attach themselves to the appropriate sites on the substrate surface
OEIC Processes - Fluidic self assembly

- Assembly of trapezoidal nanopills in matching recesses

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Magnetically Assisted Statistical Assembly

• Heterostructures grown under the optimal conditions on the optimum substrates. Close-packed pattern makes efficient use of epitaxial material.

• IC wafers can be any material: e.g. Si, SOI, GaAs, InP (even ceramic or plastic).
  - Symmetrical bilateral pills greatly simplify assembly. High symmetry, a large excess of pills, and magnetic retention insure 100% filling of wells.
  - All monolithic, batch processing features of EoE process retained; three-dimensional integration now possible (as in APB).