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High Speed Communication Circuits and Systems
Lecture 13
LNA Design Examples and Recent Techniques

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LNA Design Example

- In our previous design example, we picked the Q for the minimum possible noise factor: Q=1.4
- We (arbitrarily) chose $V_{gs}=1V$

The design yields

Noise Factor $= 1.12$ and Noise Figure $= 0.49dB$

And requires

$C_{gs} = 631 fF, L_{deg} = 0.17 nH, L_g = 12.2 nH$

$W = 392 \mu, I_{bias} = 69 mA$
Problem: the device is in velocity saturation

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MIT OCW
We Have Two “Handles” to Lower Power Dissipation

- **Key formulas**
  
  \[ I_{bias} = I_{den} W \]
  \[ F = 1 + \left( \frac{w_o}{w_t} \right) \gamma \left( \frac{g_{do}}{g_m} \right) \frac{1}{2Q} \left( 1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2 \right) \]

- **Lower current density,** \( I_{den} \)
  - **Benefits**
    \[ \Rightarrow \text{lower power, lower} \ \frac{g_{do}}{g_m} \text{ ratio} \]
  - **Negatives**
    \[ \Rightarrow \text{lower IIP3, lower} \ f_t \]

- **Lower** \( W \)
  - **Benefit:** lower power
  - **Negatives**
    \[ \Rightarrow \text{lower} \ C_{gs} = \frac{2}{3} W L C_{ox} \Rightarrow \text{higher} \ Q = \frac{1}{w_o C_{gs} 2R_s} \]
    \[ \Rightarrow \text{higher} \ F \text{ (and higher inductor values)} \]
First Step in Redesign – Lower Current Density, $I_{\text{den}}$

- Need to verify that $\text{IIP}_3$ still OK (once we know $Q$)

$V_{\text{gs}}, g_m, \text{ and } g_{\text{do}}$ versus Current Density for 0.18$\mu$ NMOS

$W/L = \frac{1.8\mu}{0.18\mu}$
Recalculate Process Parameters

- Assume that the only thing that changes is $\frac{g_m}{g_{do}}$ and $f_t$
  - From previous graph ($I_{den} = 100 \ \mu A/\mu m$)
    \[
    \frac{g_m}{g_{do}} \approx \frac{.78}{1.15} \approx 0.68 \Rightarrow \chi_d = \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}} = 0.63 \sqrt{\frac{2}{5}} \approx 0.43
    \]
    \[
    w_t \approx \frac{g_m}{C_{gs}} \approx \frac{0.78 mS}{2.9 fF} = (2\pi)42.8 \text{GHz}
    \]
- We now need to replot the Noise Factor scaling coefficient
  - Also plot over a wider range of Q

\[
F = 1 + \left(\frac{w_o}{w_t}\right) \gamma \left(\frac{g_{do}}{g_m}\right) \frac{1}{2Q} \left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right)
\]

Noise Factor scaling coefficient
Achievable values as a function of Q under the constraints that

\[ \frac{1}{\sqrt{(L_g + L_{\text{deg}})C_{gs}}} = w_0 \]

\[ \frac{g_m}{C_{gs}} L_{\text{deg}} = R_s \]

Note: \( Q = \frac{1}{2R_s w_0 C_{gs}} \)
Second Step in Redesign – Lower W (or Raise Q)

- Recall
  \[ C_{gs} = \frac{2}{3} W L C_{ox}, \quad Q = \frac{1}{w_o C_{gs} 2\beta_s} \]

- \( I_{bias} \) can be related to \( Q \) as
  \[ I_{bias} = I_{den} W = I_{den} \frac{3}{2 L C_{ox}} C_{gs} = I_{den} \frac{3}{2 L C_{ox} w_o 2\beta_s Q} \]
  \[ \Rightarrow I_{bias} \propto \frac{1}{Q} \]

- We previously chose \( Q = 1.4 \), let’s now choose \( Q = 6 \)
  - This alone cuts power dissipation by more than a factor of 4. Combined with lower \( I_{den} \), almost a factor of 8 reduction in power
  - New value of \( W \):
    \[ \Rightarrow W = 392 \mu \cdot \frac{1.4}{6} \approx 91 \mu m \]
Power Dissipation and Noise Figure of New Design

- **Power dissipation**

\[ I_{\text{bias}} = I_{\text{den}} W = (100 \mu A/\mu m)(91 \mu m) = 9.1 mA \]

- At 1.8 V supply

\[ \Rightarrow \text{Power} = (9.1 mA)(1.8V) = 16.4 mW \]

- **Noise Figure**

  - \( f_t \) previously calculated, get scaling coeff. from plot

\[ \frac{w_o}{w_t} = \frac{2\pi 1.8e9}{2\pi 42.8e9} \approx \frac{1}{23.8}, \text{ scaling coeff. } \approx 10 \]

\[ \Rightarrow \text{Noise Factor} \approx 1 + \frac{1}{23.8} 10 \approx 1.42 \]

\[ \Rightarrow \text{Noise Figure} = 10 \log(1.42) \approx 1.52 \text{ dB} \]
Updated Component Values

- Assume $R_s = 50$ Ohms, $Q = 6$, $f_o = 1.8$ GHz, $f_t = 42.8$ GHz
  - $C_{gs}$ calculated as
    \[ Q = \frac{1}{2R_s w_o C_{gs}} \]
    \[ \Rightarrow C_{gs} = \frac{1}{2R_s w_o Q} = \frac{1}{2(50)2\pi 1.8\times10^9(6)} \approx 147 \text{ fF} \]
  - $L_{deg}$ calculated as
    \[ \frac{g_m}{C_{gs}} L_{deg} = R_s \Rightarrow L_{deg} = \frac{R_s}{w_t} = \frac{50}{2\pi 42.8\times10^9} = 0.19 \text{ nH} \]
  - $L_g$ calculated as
    \[ \frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = w_o \Rightarrow L_g = \frac{1}{w_o^2 C_{gs}} - L_{deg} \]
    \[ \Rightarrow L_g = \frac{1}{(2\pi 1.8\times10^9)^2 147 \times 10^{-15}} - 0.19 \times 10^{-9} = 53 \text{ nH} \]
Inclusion of Load (Resonant Tank)

- Add output load to achieve voltage gain
  - Note: in practice, use cascode device
  - We’re ignoring $C_{gd}$ in this analysis
Calculation of Gain

- Assume load tank resonates at frequency $\omega_0$

- Assume $Z_{in} = R_s$

\[ v_{gs} = \frac{v_{in}}{2R_s} \left( \frac{1}{j\omega_0 C_{gs}} \right) = \left( \frac{Q}{j} \right) v_{in} \]

\[ i_{out} = g_m \left( \frac{Q}{j} \right) v_{in} \quad \Rightarrow \quad v_{out} = -g_m R_L \left( \frac{Q}{j} \right) v_{in} \]
**Setting of Gain**

\[ |\text{Gain}| = g_m R_L Q \]

- Parameters \( g_m \) and \( Q \) were set by Noise Figure and IIP3 considerations
  - Note that \( Q \) is of the input matching network, not the amplifier load
- \( R_L \) is the free parameter – use it to set the desired gain
  - Note that higher \( R_L \) for a given resonant frequency and capacitive load will increase \( Q_L \) (i.e., \( Q \) of the amplifier load)
    - There is a tradeoff between amplifier bandwidth and gain
  - Generally set \( R_L \) according to overall receiver noise and IIP3 requirements (higher gain is better for noise)
    - Very large gain (i.e., high \( Q_L \)) is generally avoided to minimize sensitivity to process/temp variations that will shift the center frequency and to avoid parasitic oscillation
The Issue of Package Parasitics

- Bondwire (and package) inductance causes two issues
  - Value of degeneration inductor is altered
  - Noise from other circuits couples into LNA
**Differential LNA**

- **Advantages**
  - Value of $L_{\text{deg}}$ is now much better controlled
  - Much less sensitivity to noise from other circuits

- **Disadvantages**
  - Twice the power as the single-ended version
  - Requires differential input at the chip
Note: Be Generous with Substrate Contact Placement

- Having an abundance of nearby substrate contacts helps in three ways
  - Reduces possibility of latch up issues
  - Lowers $R_{sub}$ and its associated noise
    - Impacts LNA through backgate effect ($g_{mb}$)
    - Absorbs stray electrons from other circuits that will otherwise inject noise into the LNA
  - Negative: takes up a bit extra area
Most broadband systems are not as stringent on their noise requirements as wireless counterparts.

Equivalent input voltage is often specified rather than a Noise Figure.

Typically use a resistor to achieve a broadband match to input source.
- We know from Lecture 12 that this will limit the noise figure to be higher than 3 dB.

For those cases where low Noise Figure is important, are there alternative ways to achieve a broadband match?
Recall Noise Factor Calculation for Resistor Load

- Total output noise
  \[
  \frac{v_{\text{nout}(\text{tot})}^2}{v_{\text{nout}(\text{tot})}^2} = \left(\frac{R_L}{R_s + R_L}\right)^2 \frac{e_{nRs}^2}{R_s + R_L} + \left(\frac{R_s}{R_s + R_L}\right)^2 \frac{e_{nRL}^2}{R_L}
  \]

- Total output noise due to source
  \[
  \frac{v_{\text{nout}(\text{in})}^2}{v_{\text{nout}(\text{in})}^2} = \left(\frac{R_L}{R_s + R_L}\right)^2 \frac{e_{nRs}^2}{R_s + R_L}
  \]

- Noise Factor
  \[
  F = 1 + \left(\frac{R_s}{R_L}\right)^2 \frac{e_{nRL}^2}{e_{nRs}^2} = 1 + \left(\frac{R_s}{R_L}\right)^2 \frac{4kTR_L}{4kTR_s} = 1 + \frac{R_s}{R_L}
  \]
Noise Figure For Amp with Resistor in Feedback

- **Total output noise (assume A is large and noiseless)**

\[
\frac{v_{\text{out (tot)}}^2}{v_{\text{in}}} \approx \left( -\frac{R_f}{R_s} \right)^2 e_{nR_s}^2 + e_{nR_f}^2
\]

- **Total output noise due to source (assume A is large)**

\[
\frac{v_{\text{out (in)}}^2}{v_{\text{in}}} \approx \left( -\frac{R_f}{R_s} \right)^2 e_{nR_s}^2
\]

- **Noise Factor**

\[
F \approx 1 + \left( \frac{R_s}{R_f} \right)^2 e_{nR_f}^2 = 1 + \left( \frac{R_s}{R_f} \right)^2 \frac{4kTR_f}{4kTR_s} = 1 + \frac{R_s}{R_f}
\]
Recall from Miller effect discussion that

\[ Z_{in} = \frac{Z_f}{1 - \text{gain}} = \frac{R_f}{1 + A} \]

If we choose \( Z_{in} \) to match \( R_s \), then

\[ R_f = (1 + A)Z_{in} = (1 + A)R_s \]

Therefore, Noise Figure lowered by being able to choose a large value for \( R_f \) since

\[ F \approx 1 + \frac{R_s}{R_f} \]
Resistor Termination vs. Resistor in Feedback

For Termination

\[ R_s = R_L \]
\[ F \approx 1 + \frac{R_s}{R_L} = 2 \]

For Termination

\[ R_f = (1 + A)Z_{in} = (1 + A)R_s \]
\[ F \approx 1 + \frac{R_s}{R_f} = 1 + \frac{1}{1 + A} \]
Example – Series-Shunt Amplifier

- Recall that the above amplifier was analyzed in Lecture 7
- Tom Lee’s book points out that this amplifier topology is actually used in noise figure measurement systems such as the Hewlett-Packard 8970A
  - It is likely to be a much higher performance transistor than a CMOS device, though
Recent CMOS LNA Techniques

- Consider increasing $g_m$ for a given current by using both PMOS and NMOS devices
  - Key idea: re-use of current

See A. Karanicolas, “A 2.7 V 900-MHz CMOS LNA and Mixer”, JSSC, Dec 1996
Biasing for LNA Employing Current Re-Use

- PMOS is biased using a current mirror
- NMOS current adjusted to match the PMOS current
Another Recent Approach

- Feedback from output to base of transistor provides another degree of freedom. Negative feedback improves IIP3.

For details, check out:
- Rossi, P. et. Al., “A 2.5 dB NF Direct-Conversion Receiver Front-End for HiperLan2/IEEE802.11a”, ISSCC 2004, pp. 102-103
Recent Broadband LNA Approaches

- Can create broadband matching networks using LC-ladder filter design techniques
- CMOS example:

Recent Broadband LNA Approaches (Continued)

- Bipolar example:

Gm Boosting for Noise Figure Improvement

- Gm Boosted CG Amp

\[ F = 1 + \frac{\gamma}{\alpha} \]

But, the amplifier adds noise and power. How do we boost the Gm without an amplifier?

- See Xiaoyong Li et. al., “Low-Power gm-boosted LNA and VCO Circuits in 0.18\(\mu\)m CMOS” 2005 ISSCC Digest of Technical Papers pp. 534-353

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Gm Boosting by a Transformer

- Gm is boosted without adding noise by the step-up transformer
- Transformer provides gate and source with voltages 180° out of phase: effective increase in $V_{gs}$

\[ F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1 + nk} \]
Revisit Neutralization

- Issues:
  - Power Consumption
  - Output swing (additional drop for the tail current)
  - Differential output
  - Matching between $C_{gd}$ and $C_N$
Can We Tune Out $C_{gd}$ Instead?

- Conceptually, one can tune out $C_{gd}$ by a series inductor $L$. $C_{BIG}$ is necessary to block DC between input and output.
  - Inductor value too large
  - Bottom plate parasitic capacitance of $C_{BIG}$

Neutralization by Transformer Feedback

Neutralization of $C_{gd}$ by $C_{gs}$ if

$$\frac{n}{k} = \frac{C_{gs}}{C_{gd}}$$

Advantages
- No DC drop: can operate at low supply voltages
- Power match by inductor degeneration
- No additional power consumption
- $C_{gd}$ to $C_{gs}$ matching is better than $C_{gd}$ to $C_N$
Differential Implementation

Differential Output LNA

Provides differential output to drive balanced mixers
See D. Sahu et. al. “A 90nm CMOS Single-Chip GPS Receiver with 5dBm Out-of-Band IIP3 2.0dB NF”, 2005 ISSCC Digest of Technical Papers, pp308-309

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Adjustable Gain LNA

Gain is adjusted by diverting output current in the cascode stage.

See H. Darabi, et. al, "A Fully Integrated SoC for 802.11b in 0.18\mu m CMOS", 2005 ISSCC Digest of Technical Papers, pp 96-97.