Cache Coherence Protocols
for
Sequential Consistency

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Systems view

Blocking caches
In order, one request at a time + CC ⇒ SC

Non-blocking caches
Multiple requests (different addresses) concurrently + CC ⇒ Relaxed memory models

CC ensures that all processors observe the same order of loads and stores to an address

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A System with Multiple Caches

Assumptions: Caches are organized in a hierarchical manner

- Each cache has exactly one parent but can have zero or more children
- Only a parent and its children can communicate directly
- Inclusion property is maintained between a parent and its children, i.e.,
  \[ a \in L_i \implies a \in L_{i+1} \]
Maintaining Cache Coherence

Hardware support is required such that
- only one processor at a time has write permission for a location
- no processor can load a stale copy of the location after a write

⇒

write request:
The address is invalidated in all other caches before the write is performed

read request:
If a dirty copy is found in some cache, a write-back is performed before the memory is read
Each address in a cache keeps two types of state info:

- **Sibling info**: do my siblings have a copy of address a
  - Ex (means no), Sh (means may be)
- **Children info**: has this address been passed on to any of my children
  - W(id) means child id has a writable version
  - R(dir) means only children named in the directory dir have copies
Cache State Implications

Sh $\Rightarrow$ cache’s siblings and decedents can only have Sh copies

Ex $\Rightarrow$ each ancestor of the cache must be in Ex
  $\Rightarrow$ either all children can have Sh copies
  or one child can have an Ex copy

- Once a parent gives an Ex copy to a child, the parent’s data is considered stale
- A processor cannot overwrite data in Sh state in L1
- By definition all addresses in the home are in the Ex state

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Cache State Transitions

This state diagram is helpful as long as one remembers that each transition involves cooperation of other caches and the main memory.
High-level Invariants in Protocol Design
Guardsed Atomic Actions

• Rules specified using guarded atomic actions:
  \[ \text{<guard predicate}> \rightarrow \{ \text{set of state updates that must occur atomically with respect to other rules} \} \]

• E.g.:
  \[
  m.\text{state}(a) = R(\text{dir}) \land i_d \notin \text{dir} \\
  \rightarrow m.\text{setState}(a, R(\text{dir+ id}_c)), \\
  c.\text{setState}(a, Sh); c.\text{setData}(a, m.\text{data}(a));
  \]
Data Propagation Between Caches

Caching rules
- Read caching rule
- Write caching rule

De-caching rules
- Write-back rule
- Invalidate rule

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Caching Rules: *Parent to Child*

- **Read caching rule**
  \[ R(\text{dir}) == m.\text{state}(a) \land id_c \notin \text{dir} \]
  \[ \rightarrow m.\text{setState}(a, R(\text{dir} + \text{id}_c)) \]
  \[ c.\text{setState}(a, \text{Sh}); \quad c.\text{setData}(a, m.\text{data}(a)); \]

- **Write caching rule**
  \[ \varepsilon == m.\text{state}(a) \]
  \[ \rightarrow m.\text{setState}(a, W(\text{id}_c)) \]
  \[ c.\text{setState}(a, \text{Ex}); \quad c.\text{setData}(a, m.\text{data}(a)); \]
De-caching Rules: *Child to Parent*

- **Writeback rule**
  
  \[ W(\text{id}_c) = \text{m.state}(a) \land \text{Ex} = \text{c.state}(a) \implies \text{m.setState}(a, R(\{\text{id}_c\})) \]
  
  msetData(a, c.data(a));
  c.setState(a, Sh);

- **Invalidate rule**
  
  \[ R(\text{dir}) = \text{m.state}(a) \land \text{id}_c \in \text{dir} \land \text{Sh} = \text{c.state}(a) \implies \text{m.setState}(a, R(\text{dir} - \text{id}_c)) \]
  
  c.invalidate(a);
Making the Rules *Local & Reactive*

- Some rules require observing and changing the state of multiple caches simultaneously (atomically).
  - very difficult to implement, especially if caches are separated by a network
- Each rule must be triggered by some action
- Split rules are into multiple rules – “request for an action” followed by “an action and an ack”.
  - ultimately all actions are triggered by some processor

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Protocol Design

*Note*
We will not be able to finish this part today.
(The rest of the material will be covered during the next lecture.)
Protocol Processors *an abstract view*

- Each cache has 2 pairs of queues
  - one pair (c2m, m2c) to communicate with the memory
  - one pair (p2m, m2p) to communicate with the processor
- Messages format:  
  \[ \text{msg(idsrc, iddest, cmd, priority, a, v)} \]
- FIFO messages passing between each (src, dest) pair except a Low priority (L) msg cannot block a high priority (H) msg
H and L Priority Messages

- At the memory unprocessed requests cannot block the result messages. Hence all messages are classified as H or L priority.
  - all messages carrying results are classified as high priority

- Accomplished by having separate paths for H and L priority
  - In Theory: separate networks
  - In Practice:
    - Separate Queues
    - Shared buses for both networks

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A Protocol for a system with two memory levels (L1 + M)

Cache states: Sh, Ex, Pending, Nothing
Memory states: R(dir), W(id), $T_R(dir)$, $T_W(id)$

*If dir is empty then $R(dir)$ and $T_R(dir)$ represent the same state*

Messages:
- Cache to Memory requests: ShReq, ExReq
- Memory to Cache requests: WbReq, InvReq, FlushReq
- Cache to Memory responses: WbRep(v), InvRep, FlushRep(v)
- Memory to Cache responses: ShRep(v), ExRep(v)

Operations on cache:
- cache.state(a) – returns state s
- cache.data(a) - returns data v
- cache.setState(a, s), cache.setData(a, v), cache.invalidate(a)

\[\text{inst} = \text{first(p2m)}; \text{msg} = \text{first(m2c)}; \text{mmsg} = \text{first(in)}\]
Voluntary rules: Cache must be able to evict values to create space

Invalidate rule

\[
\text{cache.state(a) is Sh} \rightarrow \text{cache.invalidate(a)}
\]
\[
c2m.enq \text{ (Msg(id, Home, InvRep, a))}
\]

Flush rule

\[
\text{cache.state(a) is Ex} \rightarrow \text{cache.invalidate(a)}
\]
\[
c2m.enq \text{ (Msg(id, Home, FlushRep, a, cache.data(v)))}
\]

Writeback rule

\[
\text{cache.state(a) is Ex} \rightarrow \text{cache.setState(a, Sh)}
\]
\[
c2m.enq \text{ (Msg(id, Home, WbRep, a, cache.data(v)))}
\]

*This rule may be applied if the cache/processor knows it is the “last store” operation to the location.*

*It would be good to have “silent drops” but difficult in a directory-based protocol*

Such voluntary rules can be used to construct adaptive protocols.
Voluntary rules: Memory should be able to send more values than requested

Cache Rule

\[ m.\text{state}(a) \text{ is } R(\text{dir}) \& \text{ id } \in \not\text{ dir} \]
\[ \rightarrow m.\text{setState}(a, R(\text{id}+\text{dir})) \]
\[ \text{out.enq} (\text{Msg(Home, id, ShRep, a, m.data(a)))) \]

*It is a rule like this that allows us to fetch locations \( a+1, a+2, \ldots \) when a processor requests address \( a \).*
Five-minute break to stretch your legs
Load Rules (at cache)

- **Load-hit rule**
  \[
  \text{Load}(a) == \text{inst} \\
  \& \; \text{cache.state}(a) \text{ is Sh or Ex} \\
  \rightarrow \; \text{p2m.deq} \\
  \text{m2p.enq(cache.data(a))}
  \]

- **Load-miss rule**
  \[
  \text{Load}(a) == \text{inst} \\
  \& \; \text{cache.state}(a) \text{ is Nothing} \\
  \rightarrow \; \text{c2m.enq(Msg(id, Home, ShReq, a))} \\
  \text{cache.setState(a,Pending)}
  \]

This is blocking cache because the Load miss rule does not remove the request from the input queue (p2m) ... more later

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Store Rules (at cache)

• Store-hit rule
  Store(a,v) == inst
  & cache.state(a) is Ex
  → p2m.deq;
  m2p.enq(Ack)
  cache.setData(a, v)

• Store-miss rules
  Store(a,v) == inst
  & cache.state(a) is Nothing
  → c2m.enq(Msg(id, Home, ExReq, a);
  cache.setState(a, Pending)

  Store(a,v) == inst
  & cache.state(a) is Sh
  → c2m.enq(Msg(id, Home, InvRep, a);
  cache.setState(a, Nothing)

Already covered by the Invalidate voluntary rule

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Processing ShReq Messages (at Home)

Uncached or Outstanding Shared Copies
Msg(id,Home,ShReq,a) == mmsg & m.state(a) is R(dir) & id \notin dir
→ in.deq;
   m.setState(a, R(dir+\{id\}));
   out.enq(Msg(Home,id,ShRep, a,m.data(a)))

Outstanding Exclusive Copy
Msg(id,Home,ShReq,a) == mmsg & m.state(a) is W(id') & (id' is not id)
→ m.setState(a, T_W(id'));
   out.enq(Msg(Home,id',WbReq, a))
Processing ExReq Messages (at home)

Uncached or cached only at the requester cache
\[
\text{Msg}(id, \text{Home}, \text{ExReq}, a) = \text{mmsg} \\
\text{& m.state(a) is R(dir) & (dir is empty or has only id)}
\rightarrow \text{in.deq} \\
\text{m.setState(a, W(id))} \\
\text{out.enq}(\text{Msg}(\text{Home}, id, \text{ExRep}, a, \text{m.data(a)}))
\]

Outstanding Shared Copies
\[
\text{Msg}(id, \text{Home}, \text{ExReq}, a) = \text{mmsg} \\
\text{& m.state(a) is R(dir) & ! (dir is empty or has only id)}
\rightarrow \text{m.setState(a, T}_R(dir\{-id\})) \\
\text{out.enq}(\text{multicast(Home, dir\{-id\}, InvReq, a})
\]

Outstanding Exclusive Copy
\[
\text{Msg}(id, \text{Home}, \text{ExReq}, a) = \text{mmsg} \\
\text{& m.state(a) is W(id') & (id' is not id)}
\rightarrow \text{m.setState(a, T}_W(id')) \\
\text{out.enq}(\text{Msg(Home, id', FlushReq, a})
\]
Processing Reply Messages (at cache)

ShRep

\[ \text{Msg(Home, id, ShRep, a, v) == msg} \]

-- cache.state(a) must be Pending or Nothing

\[ \rightarrow \text{m2c.deq} \]
\[ \text{cache.setState(a, Sh)} \]
\[ \text{cache.setData(a, v)} \]

ExRep

\[ \text{Msg(Home, id, ExRep, a, v) == msg} \]

-- cache.state(a) must be Pending or Nothing

\[ \rightarrow \text{m2c.deq} \]
\[ \text{cache.setState(a, Ex)} \]
\[ \text{cache.setData(a, v)} \]

-- In general only a part of v will be overwritten by the Store instruction.
Processing InvReq Message (at cache)

InvReq

\[
\begin{align*}
\text{Msg(Home, id, InvReq, a) }&= \text{ msg} \\
\& \; \text{cache.state(a)} \; \text{is Sh} \\
\rightarrow & \; \text{m2c.deq} \\
\text{cache.invalidate(a)} \\
\text{c2m.enq (Msg(id, Home, InvRep, a))}
\end{align*}
\]

\[
\begin{align*}
\text{Msg(Home, id, InvReq, a) }&= \text{ msg} \\
\& \; \text{cache.state(a)} \; \text{is Nothing or Pending} \\
\rightarrow & \; \text{m2c.deq}
\end{align*}
\]
Processing WbReq Message (at cache)

WbReq

\[
\text{Msg(Home, id, WbReq, a) == msg} \\
\& \quad \text{cache.state(a) is Ex} \\
\rightarrow \quad \text{m2c.deq} \\
\text{cache.setState(a, Sh)} \\
\text{c2m.enq (Msg(id, Home, WbRep, a, cache.data(v)))}
\]

\[
\text{Msg(Home, id, WbReq, a) == msg} \\
\& \quad \text{cache.state(a) is Sh or Nothing or Pending} \\
\rightarrow \quad \text{m2c.deq}
\]
Processing FlushReq Message (at cache)

FlushReq

\[\text{Msg(Home, id, FlushReq, a) == msg} \]
& cache.state(a) is Ex
\[\rightarrow \text{m2c.deq} \]
\[\text{cache.invalidate(a)} \]
\[\text{c2m.enq (Msg(id, Home, FlushRep, a, cache.data(v)))} \]

\[\text{Msg(Home, id, FlushReq, a) == msg} \]
& cache.state(a) is Sh
\[\rightarrow \text{m2c.deq} \]
\[\text{cache.invalidate(a)} \]
\[\text{c2m.enq (Msg(id, Home, InvRep, a))} \]

\[\text{Msg(Home, id, FlushReq, a) == msg} \]
& cache.state(a) is Nothing or Pending
\[. \rightarrow \text{m2c.deq} \]
Processing Reply InvRep Messages
(at home)

InvRep

\[ \text{Msg}(id, \text{Home}, \text{InvRep}, a) = mmsg \]
\[ \& \quad m.\text{state}(a) \text{ is } T_R(\text{dir}) \]
\[ \rightarrow \quad \text{deq } mmsg; \]
\[ m.\text{setState}(a, T_R(\text{dir}-\{id\})) \]

\[ \text{Msg}(id, \text{Home}, \text{InvRep}, a) = mmsg \]
\[ \& \quad m.\text{state}(a) \text{ is } R(\text{dir}) \]
\[ \rightarrow \quad \text{deq } mmsg; \]
\[ m.\text{setState}(a, R(\text{dir}-\{id\})) \]
Processing Reply WbRep Messages
(at home)

WbRep

\[
\text{Msg}(id, \text{Home}, \text{WbRep}, a, v) == \text{mmsg}
\]

-- m.state(a) must be \(T_W(id)\) or \(W(id)\)

\[\rightarrow\]

\text{deq mmsg;}

\text{m.setState}(a, \text{R}(id))

\text{m.setData}(a, v)

FlushRep

\[
\text{Msg}(id, \text{Home}, \text{FlushRep}, a, v) == \text{mmsg}
\]

-- m.state(a) must be \(T_W(id)\) or \(W(id)\)

\[\rightarrow\]

\text{deq mmsg;}

\text{m.setState}(a, \text{R}(\text{Empty}))

\text{m.setData}(a, v)
Non-Blocking Caches

- Non-blocking caches are needed to tolerate large memory latencies

- To get non-blocking property we implement p2m with 2 FIFOs (deferQ, incomingQ)

- Requests moved to deferQ when:
  - address not there
  - needed for consistency
Conclusion

• This protocol with its voluntary rules captures many other protocols that are used in practice.
  – we will discuss a bus-based version of this protocol in the next lecture

• We need policies and mechanisms to invoke voluntary rules to build truly adaptive protocols.
  – search for such policies and mechanisms in an active area of research

• Quantitative evaluation of protocols or protocol features is extremely difficult.
Thank you!
Protocol Diagram

Cache 1
Pen: $a$

ShReq $a$

Matching
Dir $a$: Sh $\{}$

Matching
Dir $a$: Sh $\{1\}$

Cache 2

Cache N

Main Memory

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Protocol Diagram

Cache 1
Pen: a
Sh: a

ShResp <a,v>

Cache 2

Cache N
...

Dir a: Sh {1}

Main Memory

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Protocol Diagram

Cache 1
Sh: \(a\)

Cache 2
Pen: \(a\)

Cache N

ShReq
\(a\)

Dir \(a\): Sh \{1\}
Dir \(a\): Sh \{1,2\}

Main Memory

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Protocol Diagram

Cache 1
Sh: a

Pen: a
Sh: a

ShResp <a,v>

Dir a: Sh {1,2}

Main Memory

Cache 2

Cache N

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Protocol Diagram
Protocol Diagram

Cache 1
- Sh: a
- Inv: a
- Dir: a: Sh {1,2}
- Dir: a: Ex {N}

Cache 2
- Sh: a
- Inv: a
- Dir: a: Sh {}

Cache N
- Pen: a
- Ex: a

Main Memory

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Protocol Diagram

Cache 1
Pen: \( a \)

ShReq \( a \)

Dir \( a: \) Ex \{N\}

Cache 2

Main Memory

Cache N
Ex: \( a \)

WBReq \( a \)

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