More CMOS circuits

MUX:

<table>
<thead>
<tr>
<th>S</th>
<th>A</th>
<th>B</th>
<th>D</th>
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<tbody>
<tr>
<td>0</td>
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Truth table for MUX

We can implement muxes with pass-transistor gates

MUX

If S is 1, the top pass gate allows A through, else the bottom gate (B) passes.
More Cross Circuits:

Register and Latches

State:
Level-sensitive closed latches:

Symbol

\[
\begin{array}{c|c|c}
D & \bar{D} & Q \\
\hline
0 & 0 & Q \\
0 & 1 & D \\
1 & 0 & D \\
1 & 1 & Q \\
\end{array}
\]

Q: Why does this work?
A: Capacitor here holds the old value long enough for the circuit to settle when \( \bar{D} = 1 \)

Brief Review of EE by analogy to水电原理

电池→电容

电阻→电阻

Using pass gate

\[
\begin{array}{c}
D \\
\hline
\bar{D} \\
\hline
\end{array}
\]

\[
\begin{array}{c}
Q \\
\hline
\bar{Q} \\
\hline
\end{array}
\]
Level sensitive Dynamic Latch.

Why bother to "restore" it with feedback?

3 a capacitor.

\[ \text{Capacitor (shown explicitly)} \]

Often 3 a lot of capacitance in one or two stages.

If \( \Phi \) runs fast enough (> 1000 Hz e.g.) then \( \Phi \) is OK.

Two-phase clocking.

Level-sensitive latches are a little tricky — cannot make

a stable minimal with that circuit.

Combination logic

When \( \Phi = 0 \) there is a loop through the C.L.
Two phase non-overlapping clocks

\[ \Phi \rightarrow \Phi_2 \rightarrow \Phi_3 \]

\[ \Phi_3 \text{ short low + } \Phi_3 \text{ low} \]

\[ \Phi_3 \text{ don't happen at the same time} \]

When \( \Phi_3 \) is low, data goes from

first latch + \( \Phi_2 \) holds its old value.

Then when \( \Phi_2 \) is low, \( \Phi_3 \) is up, so it holds the

value coming out of \( \Phi_2 \), and data flows through \( \Phi_3 \).

Will this work?

What if \( \Phi_3 \) and \( \Phi_1 \) get a little misaligned so
they cannot overlap?

It is ok if the \( \Phi_3 \) has a long enough delay

\[ \text{contamination delay} \]

or if you ensure \( \Phi_3 \) to be unoverlapping...
A array of \( N \times 2^n \) bits

\( A_0, \ldots, A_{n-1} \) names the bit \( B_i \)

at \( t+\phi \)

if \( w \) then write \( D_w \) to \( B_i \)

else \( D_{out} = B_i \)

Divide and conquer

Base case: \( n = 0 \)

\( D_{out} \)

\( A_0 \)

\( \neg \neg O \)
Analysis of RAM

Critical path:

\[ T(0) = \Theta(1) \]
\[ T(n) = 1 \text{ gate} + 1 \text{ mux} + T\left(\frac{n-1}{2}\right) \]
\[ = \Theta(n) \]
\[ = \Theta(\log N) \]

Area: Need almost

\[ \omega(n) = \Theta(1) + \omega(\Theta(n-1)) \]
\[ = \Theta(n) = \Theta(\log N) \]

Height

\[ H(n) = \Theta(1) + 2 \cdot H(n-1) \]
\[ = \Theta(2^n) - \Theta(n) \]

Q: Can we do better? Let's rethink the cost.

A: Yes, maybe...
Total width:
\[ \Theta(\sqrt{N}) + \Theta(N^{1/2} \cdot \sqrt{N}) \]

Total height:
\[ \Theta(\log N) + \Theta(\log N) \]

Total area = \[ \Theta(N \log N) \]
not better yet!
But for small \( N \) we do "wind up"

\[ \begin{align*}
\frac{5}{x} &= \frac{3}{y} \\
\text{width} &= \Theta(\sqrt{N}) \\
\text{area} &= \Theta(N)
\end{align*} \]

Two issues:

Q1) If no one drives the bus, what happens?

A: Don't care. The mux doesn't look at it.

Q2) Performance: idea to drive a bus with or taxes fine.

\[ \begin{align*}
\text{cell}_i \quad &\quad (\text{with } \text{bus}) \\
\left( \begin{array}{c}
R(\text{bus}) \\
\quad \text{transmit}
\end{array} \right)
\end{align*} \]
"Now we need to understand RC circuits."

RC circuits

\[ A \xrightarrow{RC} B \xrightarrow{C} \]

Two properties of electricity:

- Current (Amps) \( (V) \) (think current of water in a pipe)
- Voltage (Volts) \( (I) \) (think pressure or level in a pipe)

Resistor: \[ V = I \cdot R \quad \text{or} \quad \frac{V}{R} = I \] (more flow if you push harder)

Capacitor: \[ \int I \, dt = V \cdot C \]

\[ I = \frac{dV}{dt} \cdot C \]

\[ \frac{dv}{dt} = \frac{V}{RC} \]

This is a differential equation with solution of the form

\[ V = e^{\frac{-t}{RC}} \cdot e^{\frac{t}{RC}} + b \quad \text{for} \quad t > 0 \quad \text{and} \quad b \]

\[ e^{\frac{t}{RC}} + b = C \cdot e^{\frac{t}{RC}} \]

\[ \Rightarrow \quad \tau = RC \quad \text{is the time constant for the RC circuit} \]
so our circuit is:

\[ R = \Theta(1) \]
\[ C = \Theta(bn) \]

so \( \gamma = \Theta(u n) \)

next time we'll improve on this