Taxonomy of fixed-connection networks

- systolic - all state and interprocessor communication is clocked.
- semisystolic - all state is clocked.
- combinational - no state, no clocks

Finite-state machines

Moore machine

Mealy machine

A systolic network is a network of Moore machines.
A semisystolic (with no comb loops).

Example. Semisystolic palindrome recognizer
(Palindrome \( x = x^R \) (reverse))
Takes seq. \( \langle x_1, x_2, \ldots \rangle \) as input. Produces \( \langle y_1, y_2, \ldots \rangle \) as output, where

\[
y_i = \begin{cases} 1 & \text{if } x_1 x_2 \cdots x_i \text{ is a palindrome} \\ 0 & \text{otherwise} \end{cases}
\]

Eg. \( x = \langle a, b, a, c, a, b, a \rangle \)
\( y = \langle 1, 0, 1, 0, 0, 0, 1 \rangle \)
Semisystolic network
-systolic + global comb logic

$X_6 X_5 X_4 X_3 X_2 X_1$

$X_6 X_5 X_4 X_3 X_2$

$X_6 X_5 X_4 X_3$

$X_6 X_5 X_4$

$X_6 X_5$

Each cell compares its two values.
Ripple a global AND from right to left.

Real time: On same tick that $x_i$ is input, $y_i$ is output.

Only trouble: long clock period.
$\Theta(N)$ for $N$ cell array.

Abstract view of circuit
Semisystolic: ≥0 registers on each edge
Systolic: ≥1 register on each edge

Transformation techniques

1. Slowdown: Double register counts

Same function as original semisystolic circuit, but clock twice.

2. Retime

Systolic! Same functionality as doubled semisystolic circuit, but no long comb delays.
- Initialization may differ.
Retiming a node

\[ \text{lag of } r(v) = k \quad \text{lag of } r(v) = -k \]

Retimed edge weights must be \( \geq 0 \).

\[ w_r(e) = w(e) - r(u) + r(v) \]

**Def.** Let \( G = (V, E, w) \) be edge-weighted digraph, where \( w(e) \geq 0 \) \( \forall e \in E \). A retiming of \( G \) is a mapping \( r : V \rightarrow \mathbb{Z} \). The retimed graph is \( G_r = (V, E, w_r) \), where \( w_r(e) = w(e) - r(u) + r(v) \) \( \forall e \in E \). The retiming is legal if \( w_r(e) \geq 0 \) \( \forall e \in E \).

Note: Normally, we assume \( r(\text{Host}) = 0 \).
Lemma. Let $G = (V, E, w)$ be a circuit, and let $r : V \rightarrow \mathbb{Z}$ be refining. Then, for any path $u \rightarrow v$ in $G$, we have

$$w_r(p) = w(p) - r(u) + r(v).$$

Pf. Suppose $p$ is $V_0 \xrightarrow{e_0} V_1 \xrightarrow{e_1} \cdots \xrightarrow{e_{k-1}} V_k$.

$$w_r(p) = \sum_{i=0}^{k-1} w_r(e_i)$$

$$= \sum_{i=0}^{k-1} (w(e_i) - r(v_i) + r(v_{i+1}))$$

$$= \sum_{i=0}^{k-1} w(e_i) + \sum_{i=0}^{k-1} (-r(v_i) + r(v_{i+1}))$$

$$= w(p) - r(v_0) + r(v_k) \quad \text{(telescope)} \quad \blacksquare$$

Corollary. For any cycle $p$, $w_r(p) = w(p)$. \quad \blacksquare$

Theorem (Systolic conversion)

Let $G = (V, E, w)$ be a semisystolic circuit, and define $G^{-1} = (V, E, w')$, where $w'(e) = w(e) - 1$ for $e \in E$. Then, there is a legal refining $r : V \rightarrow \mathbb{Z}$ of $G$ such that $G^r$ is systolic iff $G^{-1}$ has no negative-weight cycles.

the “constraint graph”
Example:

\[ G \]

\[
\begin{array}{c}
\text{Host} \\
\end{array}
\]

\[ G'-1 \]

\[
\begin{array}{c}
\text{Host} \\
\end{array}
\]

\[ \text{No neg.-wtx cycles.} \]

Proof:

\((\Leftarrow)\) Suppose \( G'-1 \) has no neg.-wtx cycles.

Define \( r(v) = w^+ \) of shortest path from \( v \) to host in \( G'-1 \).

Note: \( r(v) \) defined, since \( G'-1 \) has no neg.-wtx cycles.

Claim: \( \forall u \neq v \in E, \; w_{r}(e) = w(e) - r(u) + r(v) \geq 1 \).

\[ \Delta \text{-ineq.:} \quad r(u) \leq w(e)-1 + r(v) \]

\[ \frac{\text{sh. path from } u \text{ in } G'-1}{\text{wt. of } e \text{ in } G'-1} \quad \frac{\text{sh. path from } v \text{ in } G'-1}{\text{sh. path in } G'-1} \]

Rewrite: \( w_{r}(e) = w(e) - r(u) + r(v) \geq 1 \).
(⇐) Sup. \( G - 1 \) has neg. wt cycle \( v_0^{e_0} \rightarrow v_1^{e_1} \rightarrow \ldots \rightarrow v_k^{e_k} \rightarrow v_0 \)

Then \( \sum_{i=0}^{k} (\omega(e_i) - 1) < 0 \)

\[ \Rightarrow \sum_{i=0}^{k} \omega(e_i) < k. \]

But, \( \sum_{i=0}^{k} \omega_r(e_i) \geq k \), and \( \sum_{i=0}^{k} \omega_r(e_i) = \sum_{i=0}^{k} \omega(e_i) \).

Contradiction. □