We've given you a lot of tricks for understanding feedback systems when they are given to us as a block diagram. Sometimes, getting a feedback system from its “physical” form as a schematic diagram to block diagram form is a bit of an art. This “art” is greatly enhanced by the use of thoughtful approximations.

One such approximation you've already seen:

![Op-Amp Diagram]

We can either do the math, or reason in the following way: since the gain of the op-amp is huge, the voltage at v- must be very small for ordinary values of v_o. We decide to call v- a virtual ground, and then crank merrily along.

This type of thinking helps tremendously in analyzing complicated circuits like op-amps. Let's look and see how.
CLASS EXERCISE

Consider the following two feedback circuits:

Diagram 1.

Diagram 2.

For each, determine \( \frac{v_o}{i_{IN}} \) in the limit of \( A \gg 1 \). Also determine \( v_i \) in each case.

(Workspace below)

Notice that these are feedback systems, even though the summing junction doesn’t leap out at you. A valid block diagram for circuit (2) is (in the limit of large \( A \)):
Anyway, the key idea is that when the gain $A$ is large, $v_{IN}$ becomes a virtual ground. So how large is large enough?

Depends on the accuracy you want, but let's try out some numbers to help clarify what we're dealing with. Suppose that $A = 10$, and we're calculating the current through the feedback element.

\[
\text{Actual } I_t : \quad \frac{-\frac{1}{10} V_O - V_O}{R_f} = \frac{-\frac{11}{10} V_O}{R_f}
\]

\[
\text{Approximating } 10 \approx \infty : \quad I_t = \frac{-V_O}{R_f}
\]

Even with the gross approx. $10 \approx \infty$, we're only off by about 10%.

These numbers should help to give you a feel for why we're not punished for making what seem like horrendous approximations.

The idea behind all of this is to help you understand the op-amp analysis that we've started in lecture.
An Op-Amp example:

Writing node equations to analyze this circuit is a major, major pain. But with some thoughtful approximating, understanding this circuit can be made much easier.

Start by redrawing:
Now the gain stage provides a gain well in excess of 10. Recognizing this helps us to understand this circuit as an example of minor-loop compensation.

The current through $C_c$ is just:

$$I_c = sC_c v_o$$

We can replace the capacitor $C_c$ with the ideal block

$$\begin{array}{c}
\text{I}_c \\
\text{sC}_c \\
\text{v}_o
\end{array}$$

...provided we properly account for capacitive loading effects.

Define

$$C_3 = C_1 + \frac{C_2 C_c}{C_2 + C_c}$$

$$C_4 = C_2 + C$$

Following things through to the end, we wind up with a block diagram that looks like:
Believe it or not, a straight algebraic approach will eventually lead you here. Analyzing things this way gets you here much faster, though, and with a clearer understanding of what is going on.