Problem Set #2: Updates and Frequently Asked Questions

Notes and Hints:

Problem 6:

- *** The expression for $S$ should be read as $S=ABC+(A\cdot\neg B\cdot\neg C)+(\neg A\cdot\neg B\cdot C)+(\neg A\cdot B\cdot\neg C)$. If you interpreted it as $A\cdot\neg(BC)$ etc and have already completed the layout we'll accept that, but please complete the other parts of the problem for the correct interpretation of $S$.
- This should read just "transmission gate", not "NMOS transmission gate" You may assume inputs and their complements are available as inputs.
- For part c, the sizing should be $W/L=0.5/0.25\mu$ for all NMOS and $W/L=2\mu/0.25\mu$ for all PMOS.