1. The following is based on Problem 5 in Chapter 11 of Thomas Lee’s book. Consider the resistively shunted amplifier shown in Figure 1. $V_{dd}=1.8$ volts, $I_{bias}=200\mu A$, $R_L=1k\Omega$.

![Amplifier Circuit Diagram](image.png)

Figure 1: Amplifier with resistive input termination.

(a) Assuming all transistors are in saturation:

i. What voltage is $V_{out}$ biased at? How much current flows through $M_2$?

ii. Using Hspice, find $g_m$ and $C_{gs}$ for $M_1$ with 0.18 $\mu m$ Hspice model file provided in Athena in the file /mit/6.976/Models/0.18u/mos018.mod.

(b) Assuming that $C_{big1}$ and $C_{big2}$ are short circuits at the frequencies of interest, redraw a simplified version Figure 1 for calculating the noise figure of the amplifier.
(c) Given the assumption in part (b), does the bias transistor $M_2$ impact the noise figure of the amplifier?

(d) Derive an expression for the noise figure (factor) of the amplifier. Assume that all transistors are in saturation, and ignore the impact of gate noise, $C_{gd}$, $r_o$, and source/drain capacitances in $M_2$. Also assume for $M_2$ that

$$\overline{v_{nd}^2} = 4kT\gamma g_{do}\Delta f,$$

$$g_m/C_{gs} = w_T,$$

where the excess noise factor $\gamma = 3$ and $\alpha = 0.5$.

(e) Based on your expression in part (d):

i. Is the noise figure a function of frequency? If so, is the noise performance of the amplifier better at high or low frequencies?

ii. Is the noise figure of the amplifier minimized for $R_T \ll 50\Omega$, $R_T = 50\Omega$, or $R_T \gg 50\Omega$?

iii. What is the minimum noise figure that can be achieved with $w_T/w = 10$?

iv. What is the noise figure for $R_T = 50\Omega$ with $w_T/w = 10$?

(f) Rederive the expression for noise figure (factor) of the amplifier under the same conditions as in part (d) except that you should now include the impact of gate noise. Assume that the gate noise is described as:

$$\overline{i_{ng}^2} = 4kT\delta g_g\Delta f,$$

where the gate noise coefficient $\delta = 6$. Also assume that gate noise is correlated with drain noise as:

$$c = \frac{\overline{i_{ng}^2 \cdot i_{nd}^2}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} = j0.55$$

(g) Is the noise figure a function of frequency? If so, is the noise performance of the amplifier better at high or low frequencies?

(h) What is the noise figure for $R_T = 50\Omega$, $w_T/w = 10$?
2. Now consider the resistively shunted amplifier employing a cascode transistor as shown in Figure 2. For the questions below, assume that all transistors are in saturation and $\omega \ll \omega_T$. Ignore the impact of gate noise, $C_{gd}$, $r_o$, and source/drain capacitances in $M_2$ and $M_3$. Also assume for $M_2$ and $M_3$ that

$$\bar{I}_{nd}^2 = 4kT \gamma g_{do} \Delta f, \quad g_m/C_{gs} = w_T,$$

\[\text{Figure 2: Cascoded amplifier with resistive input termination.}\]

(a) From an intuitive perspective, what is the impact of $M_3$ on the overall noise figure of the amplifier if $C_{par} = 0$? Justify your answer.

(b) Also from an intuitive perspective, how does $C_{par}$ impact the overall noise figure as its value is increased above zero? Justify your answer.

(c) Derive an expression for the noise figure (factor) of the cascoded amplifier assuming $C_{par}$ is nonzero.

3. This problem focuses on estimating IIP3 and IIP2 for the single-ended and differential amplifiers shown in Figure 3.

(a) Enter each of the circuits into Cadence and perform a DC sweep using Hspice for each one as follows:

i. Circuit (a): sweep $V_{in}$ over the range of -10 mV to 10 mV. Be sure to probe node $V_{out}$.

ii. Circuit (b): sweep $V_{id}$ over the range of -20 mV to 20 mV. Be sure to probe node $V_{od}$.

(b) Use Matlab to curve fit a third order polynomial to each of the Hspice plots obtained in part (a). Specifically, derive the coefficients for the following polynomials:
Figure 3: Example amplifiers for nonlinearity analysis: (a) single-ended, (b) differential.

i. Circuit (a): \( V_{out} \approx c_0 + c_1 V_{in} + c_2 V_{in}^2 + c_3 V_{in}^3 \),

ii. Circuit (b): \( V_{od} \approx c_0 + c_1 V_{id} + c_2 V_{id}^2 + c_3 V_{id}^3 \).

To do so, create matrices (for circuit (a) in this case):

\[
y = \begin{bmatrix}
V_{out}[i] \\
V_{out}[i+1]
\end{bmatrix}, \quad A = \begin{bmatrix}
\vdots & \vdots & \vdots & \vdots & \vdots \\
1 & V_{in}[i] & V_{in}^2[i] & V_{in}^3[i] \\
1 & V_{in}[i+1] & V_{in}^2[i+1] & V_{in}^3[i+1] \\
\vdots & \vdots & \vdots & \vdots & \vdots
\end{bmatrix}, \quad h = \begin{bmatrix}
c_0 \\
c_1 \\
c_2 \\
c_3
\end{bmatrix}
\]

so that we have the matrix relationship:

\[ y = Ah. \]

We solve for the coefficients in vector \( h \) using the least squares technique by using the Matlab command:

\[ h = A\backslash y \]

(c) Plot the calculated polynomial versus the Hspice computed curves for \( V_{out} \) and \( V_{od} \) over the range of \( V_{in} \) and \( V_{id} \), respectively, specified in part (a). How well does the polynomial match its respective simulation curve?

(d) Given the computed coefficients from part (b), calculate IIP3 for both amplifiers assuming that the amplifiers are shunt loaded at their inputs with a 50 \( \Omega \) resistor, and are also driven by a source with 50 \( \Omega \) source resistance (just as in problems (1), (2) and (4)). Does one have higher IIP3 than the other? If so, why?

(e) Given the computed coefficients from part (b), calculate IIP2 for both amplifiers under the same assumptions as in part (c). Does one have higher IIP2 than the other? If so, why?
4. In this problem we will use CppSim to “experimentally” calculate IIP3 of the amplifier shown in Figure 4. Assume that:

\[ c_0 = .5, c_1 = 1, c_2 = .03, c_3 = -.07 \]

![Amplifier configuration for CppSim Simulation.](image)

**Figure 4:** Amplifier configuration for CppSim Simulation.

(a) What is the theoretical value of IIP3 of the amplifier given the coefficients above?

(b) Create an amplifier module symbol and schematic in CppSim that contains parameters for \( c_0 \), \( c_1 \), \( c_2 \), and \( c_3 \). Create a corresponding module entry in the modules.par file that implements the amplifier using the Amp class. Refer to /mit/CppSim/Doc/cppsimdoc.pdf for Amp Class usage and creating modules in Cadence. Turn in the module symbol and code for Amp.

(c) Create a gain module symbol and schematic in CppSim that contains a parameter for the gain value. Set up the parameters so that you use the gain module already in modules.par. Turn in the module symbol.

(d) Create a schematic in Cadence using the above modules as shown in Figure 5. Set the signal_source signal type to a sine wave of frequency 1 GHz. Create a test.par file corresponding to the circuit that specifies a sample rate of 50 GHz and the number of sample points as 10000.

![CppSim schematic for IIP3 computation.](image)

**Figure 5:** CppSim schematic for IIP3 computation.

Now, “experimentally” calculate IIP3 for the amplifier by adjusting the gain value over several appropriately chosen values and then measuring the resulting fundamental and third order distortion products (observe these products by taking the fft of the output of the amplifier and then measuring the appropriate tone amplitudes in the frequency domain). Does your IIP3 estimate agree with the theoretical calculation in part (a)? (NOTE: in the future, do this as a two tone test rather than a one tone test)