RF Power Amplifiers

May 7, 2003
Outline

- **PA Introduction**
  - Power transfer characteristics
  - Intrinsic PA metrics
  - Linear and Non-linear amplifiers
  - PA Architectures

- **Single-Stage Linear PA**
  - Load-line theory
  - Transistors size
  - Input and Output Matching
  - So why is this so hard?

- **High-efficiency PAs**
  - Class A, AB, B and C amplifiers
Outline (cont.)

- **Real-World Design Example**
  - Selecting architecture, number of stages
  - Designing stages
  - Tuning: inter-stage match and output

- **System specifications**
  - Ruggedness: load mis-match and VSWR
  - Linearity: spectral mask (ACPR), switching transients
  - Noise in receive band

- **Power Control**
PA Transfer characteristics

Defining linearity:

\[ P_{out} = P_{in} + G \]

linear

non-linear (actual)
PA Transfer characteristics

Defining linearity:

\[ G = \frac{P_{\text{out}}}{P_{\text{in}}} \]

- \( P_{\text{MAX}} \)
- \( P_{1\text{dB}} \)

Gain (dB)

\( P_{\text{out}} \) (dBm)

\( P_{\text{in}} \) (dBm)
PA Introduction: Intrinsic PA Metrics

- $P_{1\text{dB}}$: Output power at which linear gain has compressed by 1dB (measure of linear power handling)
- $P_{\text{MAX}}$: Maximum output power (saturated power)
- Gain: Generally taken to mean transducer gain

\[
\text{Power delivered to load} \quad \frac{\text{Power available from source}}{\text{Power to load} - \text{Power from source}}
\]

- PAE: Power-added Efficiency

\[
\text{Power to load} - \text{Power from source} \quad \frac{\text{Power from supply}}{\text{Power from supply}}
\]
Linear and Non-linear PAs

- “Linear PA” generally refers to a PA which operates at constant gain, needs to preserve amplitude information.

\[ \text{POUT (dBm)} \]
\[ \text{PIN (dBm)} \]

- Not necessarily class A (will discuss later …) Peak efficiencies often only 40 to 45 %
- Useful for modulation schemes with amplitude modulation (QPSK, 8-PSK, QAM)
Linear and Non-linear PAs

“Non-linear PA” generally refers to a PA designed to operate with constant $P_{IN}$, output power varies by changing gain.

- Operation in saturated mode leads to high peak efficiencies $> 50$%; “backed-off” efficiencies drop quickly.
- Useful for constant-envelope modulation schemes (GMSK).

![Graph showing $P_{OUT}$ vs $P_{IN}$](image)

Designed to operate here: NOT fixed gain! $P_{OUT}$ adjusted through bias control.
**PA Architectures**

Typical 2-stage (6.012) design

![Circuit Diagram](image)

- **$V_{POS}$**
- **$I_{REF}$**
- **$V_{B1}$**
- **$V_{B2}$**
- **50 $\Omega$**

**Max power transfer?**

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“RF IF” logo is visible in the top left corner and “ANALOG DEVICES” logo is visible in the bottom right corner.
**PA Architectures**

Typical 2-stage RF PA design

- **$V_{POS}$**
- **RF input**
- **$V_{B1}$**
- **$V_{B2}$**
- **Matching network**
- **50 $\Omega$**

**Inductive RF choke** allows output to rise above $V_{POS}$, doesn’t dissipate power.

L’s and C’s to transform load impedance.

May require additional RF choke here to isolate input from bias circuit.
PA Architectures

Typical 2-stage RF PA design

Additional caps may be required for matching network, harmonic termination
PA Architectures

Typical 2-stage RF PA design

$V_{\text{POS}}$

RF input

$V_{\text{B1}}$

$V_{\text{B2}}$

matching network

matching network

50 Ω

bond wires (at least …)
PA Architectures

Typical 2-stage RF PA design

Consider this …
PA Architectures

- “Gain stage” is one transistor with passive elements
- “Active” components often limited to 2 or 3 transistors (gain stages) in signal path
- Transistor design very important!
  - Many parallel transistors – often look like mini-circuits themselves
- Passive components just as important as transistors!
  - Circuits must be tunable to account for uncertainties in determining values *a priori* (i.e. simulations stink – especially large-signal, RF simulations)
  - Q and parasitic elements of passives important
Single-Stage Linear PA

- Load-line theory: the maximum power that a given transistor can deliver is determined by the power supply voltage and the maximum current of the transistor

\[
R_{LOAD,\text{opt.}} \approx \frac{2 \cdot V_{POS}}{I_{MAX}}
\]
Single-Stage Linear PA

- Transistor size chosen to deliver required output power

\[ P_{OUT} \approx I_{MAX} \cdot V_{POS} / 4 \]
**Single-Stage, Linear PA**

- Design output match to transform 50Ω load to $R_{L,\text{opt}}$ at transistor output; then design input match for gain (complex conjugate)

```
V_{\text{POS}}
```

- Circuit diagram showing input match and output match with $V_{B1}$ and 50 Ω load.
Seems simple, so why is this so hard?

- Determining $I_{\text{MAX}}$ is not so easy
  - For BJT's, one reference suggested that “the best way of estimating its value is to build an optimized class A amplifier and observe the dc supply current.”\(^1\)
  - Somewhat easier for depletion-mode GaAs FETs – $I_{\text{MAX}}$ often corresponds to $V_{GS} = 0\text{V}$
  - Values don’t scale linearly with transistor size

- Optimal load resistance only a theoretical number
  - Transmission line effects, parasitic L’s and C’s significant at RF
  - Common practice is to vary the load of an actual transistor to determine the peak output power: the load-pull measurement
    (Noticing a distinct pattern of “empirical” design emerging?)

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\(^1\) RF Power Amplifiers for Wireless Communications, Steve Cripps, Artech House, Boston, 1999.
Seems simple, so why is this so hard?

- Now consider the problem for multiple stages ... double the trouble
  - Typical single-stage gain only 10 – 15 dB
  - Inter-stage match now required to match input impedance of 2\textsuperscript{nd} stage to desired output impedance of 1\textsuperscript{st} stage.

- Problems with matching circuits:
  - Large matching ratios $\rightarrow$ high Q circuits for simple L matches
  - Multi-segment matches use valuable real estate, add cost

- Transistor itself matters – a lot!
  - Many parallel transistor
  - Ballasting, balancing and layout extremely important
High-efficiency PAs

- Input signal swing turns on transistor – conduction for only part of sinusoidal period

![Graph showing the relationship between $I_D$ or $I_C$ (mA/mm), $V_{DS}$ or $V_{CE}$ (V), and the quiescent point moving from Class A to Class AB to B.](image-url)
**High-Efficiency PAs**

Class A:

\[ \alpha = 2\pi \]

Class AB:

\[ \pi < \alpha < 2\pi \]

Class B:

\[ \alpha = \pi \]

Class C: \( \alpha < \pi \)
High-Efficiency PAs

- Assume output match will filter out non-linearities caused by discontinuous conduction:

![Diagram showing input match and output match with 50Ω transformed to R_{L,\text{opt}}. All harmonics filtered out.](image)
High-Efficiency PAs

- If all harmonics filtered out, then voltage output at load is a pure sinusoid, despite discontinuous conduction

![Diagram showing voltage output (V_OUT) and current (I_MAX) over time (ωt)]

- Energy stored in reactive elements delivers current to the load during transistor off-portion of cycle
High-Efficiency PAs

- Now consider peak efficiencies

Calculate fundamental component of current*

\[
I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} I_Q + I_{pk} \cos(\omega t) \, d\omega t
\]

\[
I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} I_{pk} \cos(\omega t) \cos(n\omega t) \, d\omega t
\]

* There are many texts which cover reduced-conduction angle calculations. See for example *Principles Of Power Electronics*, Kassakian, Schelcth and Verghese, Ch. 3.
High-Efficiency PAs

From phasor plot: \[ \cos(\alpha/2) = -\frac{I_Q}{I_{pk}} = -\frac{I_Q}{(I_{MAX} - I_Q)} \]

Put it all together and do the math, you get:

\[ I_{dc} = \frac{I_{MAX}}{2\pi} \frac{2\sin(\alpha/2) - \alpha \cos(\alpha/2)}{1 - \cos(\alpha/2)} \]

\[ I_{1,0-p} = \frac{I_{MAX}}{2\pi} \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)} \]

Assume \( V_{OUT} \) the same for all classes:

\[ V_{1,0-p} = V_{POS} \]
High-Efficiency PAs

- Summary of PA “ideal” peak efficiencies

Class A:
\[
\frac{P_I}{P_{dc}} = \frac{(I_{MAX}/2)/\sqrt{2} \cdot V_{POS}/\sqrt{2}}{(I_{MAX}/2) \cdot V_{POS}} = 50 \%
\]

Class B:
\[
\frac{P_I}{P_{dc}} = \frac{(I_{MAX}/2)/\sqrt{2} \cdot V_{POS}/\sqrt{2}}{(I_{MAX}/\pi) \cdot V_{POS}} = 78 \%
\]

Class C: Ideally can go to 100%, but $P_1$ drops steadily beyond $\alpha=\pi$, goes to 0 at 100%!
High-Efficiency PAs

- What happened to our load line?
  - For class B fundamental $R_{L,\text{opt}} = \frac{V_{\text{POS}}}{I_{\text{MAX}}/2}$ – Didn’t change

![Diagram showing load lines for Class A and Class B]

Class B is here! $V_{DS}$ or $V_{CE}$ (V)
High-Efficiency PAs

- What happened to our load line?
  - For class B fundamental $R_{L,\text{opt}} = \frac{V_{\text{POS}}}{(I_{\text{MAX}}/2)}$ – Didn’t change

In quasi-static picture, resistance presented to transistor output cut in half. But average resistance is the same for class A.
High-Efficiency PAs

- Now consider “linearity”
  - Clearly the current waveforms are far from linear

BUT ...

- Overall $P_{OUT}$ vs. $P_{IN}$ transfer function can still be quite linear, especially for true Class B where output current waveform is symmetrical with respect to input waveform

Because conduction angle is constant, $P_{OUT}$ changes proportional to $P_{IN}$
Real-World Design Example

- **IDEAL:** Design each stage independently
  - Determine required gain – number of stages
  - Determine $P_{\text{OUT}}$ for each stage
  - Determine $R_{L,\text{opt}}$ for each stage
  - Determine input impedance for each stage
  - Design matching networks for inter-stage, load and input

- **REALITY:**
  - $I_{\text{MAX}}$ doesn’t scale nicely with transistor size. Without good $I_{\text{MAX}}$ numbers, can’t determine $R_{L,\text{opt}}$. Need to do load-pull.
  - Even load pull measurements have limited accuracy for very large transistors
  - Designs are very empirically driven!
Real-World Design Example

GSM 900 MHz, GaAs HBT PA Design

- \( P_{\text{OUT}} = 33 \text{ dBm} \) (linear) = 2 W
- \( V_{\text{CC}} = 3.5\text{V} \)
- \( R_{\text{LOAD}} = \frac{V_{\text{CC}}^2}{2 \times P_{\text{OUT}}} = 3 \Omega \)
- \( I_{\text{MAX}} = \frac{2 \times V_{\text{CC}}}{R_{\text{LOAD}}} = 2.33 \text{ A} \)
  (Note: expect saturated power to be \( \sim 35 \text{ dBm} \))

- Input power: constant-envelope +5 dBm
- Gain = \( P_{\text{OUT}} - P_{\text{IN}} = 27 \text{ dB} \).
- Expect roughly 10 dB per stage

3 STAGE DESIGN
Real-World Design Example

- **Stage 1**: Gain = 10 dB → $P_{\text{OUT}} = 15 \text{ dBm}$
  - $R_{L1} = \frac{V_{CC}^2}{2*P_{\text{OUT}}} = 194 \Omega$
  - $I_{\text{MAX}} = \frac{2*V_{CC}}{R_{\text{LOAD}}} = 36 \text{ mA}$
  - Chose class A: $I_{\text{DC}} = \frac{I_{\text{MAX}}}{2} = 18 \text{ mA}$
    (18 mA insignificant compared to 2.33 A)
- **Stage 2**: Gain = 10 dB → $P_{\text{OUT}} = 25 \text{ dBm}$
  - $R_{L2} = 19.4 \Omega$
  - $I_{\text{MAX}} = 360 \text{ mA}$
  - Still probably class A (maybe AB): $I_{\text{DC}} = \frac{I_{\text{MAX}}}{2} = 180 \text{ mA}$
- **Stage 3**: Gain = 7 dB → $P_{\text{OUT}} = 33 \text{ dBm}$
  - $R_{L2} = 3 \Omega$, $I_{\text{MAX}} = 2.33 \text{ A}$
  - Class B: $I_{\text{DC}} = \frac{I_{\text{MAX}}}{\pi} = 742 \text{ mA}$
A note on “Gain”

- Taking a very simplistic view of common emitter stages:
  - \( g_{m1} = \frac{I_C}{V_{Th}} = \frac{18 \text{ mA}}{0.025 \text{ V}} = 0.696 \text{ S} \)
  - \( g_{m1}R_L = 0.696 \cdot 194 = 135 \rightarrow \text{NOT 10 dB!} \)

BUT ...

- \( r_e1 = \frac{1}{g_{m1}} = 1.44 \Omega \)
- \( r_e2 = \frac{1}{g_{m2}} = 0.144 \Omega \)
- \( r_e3 = \frac{1}{g_{m3}} = 0.035 \Omega \)

1. Remember it’s power gain, not voltage gain. Can lose voltage at input match.
2. It’s pretty tough not to get significant degeneration!
Real-World Design Example

- Efficiency calculations:
  - $I_{DC1} = 18 \text{ mA}$, $I_{DC2} = 180 \text{ mA}$, $I_{DC3} = 742 \text{ mA}$
  - Total DC Current: 940 mA

\[
\frac{P_I}{P_{dc}} = \frac{(I_{MAX}/2)/\sqrt{2} \cdot V_{POS}/\sqrt{2}}{I_{DC} \cdot V_{POS}} = 62 \%
\]

- Realistically may get as high as 55%
Real-World Design Example: Load-Pull

- After initial “guesses” at transistor sizes, load-pull to determine actual target load for matching circuits

Load pull: Vary $Z_L$
Plot contours of constant power

$P_{MAX}$
$P_{MAX} - 1\text{dB}$
$P_{MAX} - 2\text{dB}$
Real-World Design Example: Load-pull

Notes on load-pulling:
- Most accurate on probe station, but insertion loss of probes prevents it from being useful for large transistors ("Insertion loss" is RF code word for resistance)
- Bonded devices on evaluation board must be carefully de-embedded
- Even using electronic tuners, accuracy is poor for very large transistor (i.e. for loads in the $2 – 5 \, \Omega$ range)
Real-World Design Example: The Circuit

GaAs die

RF input

$V_{B1}$

$V_{B2}$

$V_{POS}$

50 Ω
Real-World Design Example: The Circuit
Real-World Design Example

\[ V_{\text{POS}} \]

\[ L_{\text{BOND}} + TL \]

\[ L_{\text{BOND}} + TL \]

\[ L_{\text{BOND}} + L_{\text{VIA}} \]

RF input

\[ V_{B1} \]

\[ V_{B2} \]

printed inductor

50 Ω

\[ L_{\text{parasitic}} + L_{\text{VIA}} \]
Real-World Design Example

$V_{POS}$

RF input

may need to add feedback for stability

$V_{B1}$

$V_{B2}$

$V_{B2}$

50 Ω
Real-World Design Example: Tuning

- Example of inter-stage match, 1\textsuperscript{st} to 2\textsuperscript{nd} stage

\[ R_{L1} = 194 \ \Omega \ (?) \]
\[ Z_{IN2} = 30 - j10 \ (?) \]

Both are really just guesses

* Go to Winsmith: test
Real-World Design Example: Tuning

Example of inter-stage match, 2\textsuperscript{nd} to 3\textsuperscript{rd} stage

\[ R_{L2} = 19.4 \ \Omega \]
\[ Z_{IN3} = 2 - j2 \]

* Go to Winsmith: test2
System Specifications

- **Ruggedness**
  - 50 Ω load is for antenna in free space. Place antenna on a metal plate and can easily get VSWR of 4:1.
  - Typical PA specs are: don’t oscillate at up to 4:1, survive up to 10:1 (!)

\[
\begin{align*}
V_1^- &= \Gamma \cdot V_1^+ \\
V_1^+ &= V_1^- \\
\end{align*}
\]

\[t = t_1\]

\[t = t_2\]
System Specifications

- **Linearity**
  - For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important

![raised cosine filter diagram]

- Power Spectral Density (PSD) (dBm/Hz)
- freq. $f_c - \Delta f$, $f_c$, $f_c + \Delta f$
- ch. A, B, C
System Specifications

- **Linearity**
  - For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important

![Diagram](image)

- **Power Spectral Density (PSD)** (dBm/Hz)
- **3rd order distortion**

- Channels: A, B, C

- Frequency: $f_c$, $f_c - \Delta f$, $f_c + \Delta f$
System Specifications

- **Linearity**
  - For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important

![Diagram showing Power Spectral Density (PSD) with channels A, B, and C, illustrating 3rd and 5th order distortion regions. The diagram includes frequency axes labeled $f_c - \Delta f$, $f_c$, and $f_c + \Delta f$.](image)
System Specifications

◆ Linearity
  ● For linear PAs, Adjacent Channel Power Ratio (ACPR) is very important

$$\text{ACPR} = \frac{\text{Pwr. Ch. B}}{\text{Pwr. Ch. A}}$$
System Specifications

- **Linearity**
  - For non-linear PA in TDMA systems, harmonic spurs and switching transients are most common measure of linearity

![Diagram showing signal ramping profile and 577μs GSM burst. Signal ramping profile must fall within time mask.](image)
System Specifications

- Noise in receive band:
  - Obvious spec. in systems where Tx and Rx are operating at the same time (FDD)
System Specifications

- Noise in receive band:
  - Obvious spec. in systems where Tx and Rx are operating at the same time (FDD)
  - Not so obvious spec in TDD system. Problem primarily of mixing by the PA ($2\omega_2 - \omega_1$ or $\omega_2 - \omega_1$)}
Power Control

- For linear PA, expected to operate at constant gain. Power control is therefore a function of $P_{\text{IN}}$.
- Role of bias circuitry is to maintain constant gain over $P_{\text{IN}}$, temperature (PTAT?).

![Power transistor diagram]
Power Control

For non-linear PA, expected to operate at constant $P_{\text{IN}}$. Power control is achieved by varying gain.

External control signal $V_{\text{APC}}$

On-chip bias circuitry

Power transistor