RF Power Amplifiers

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Outline

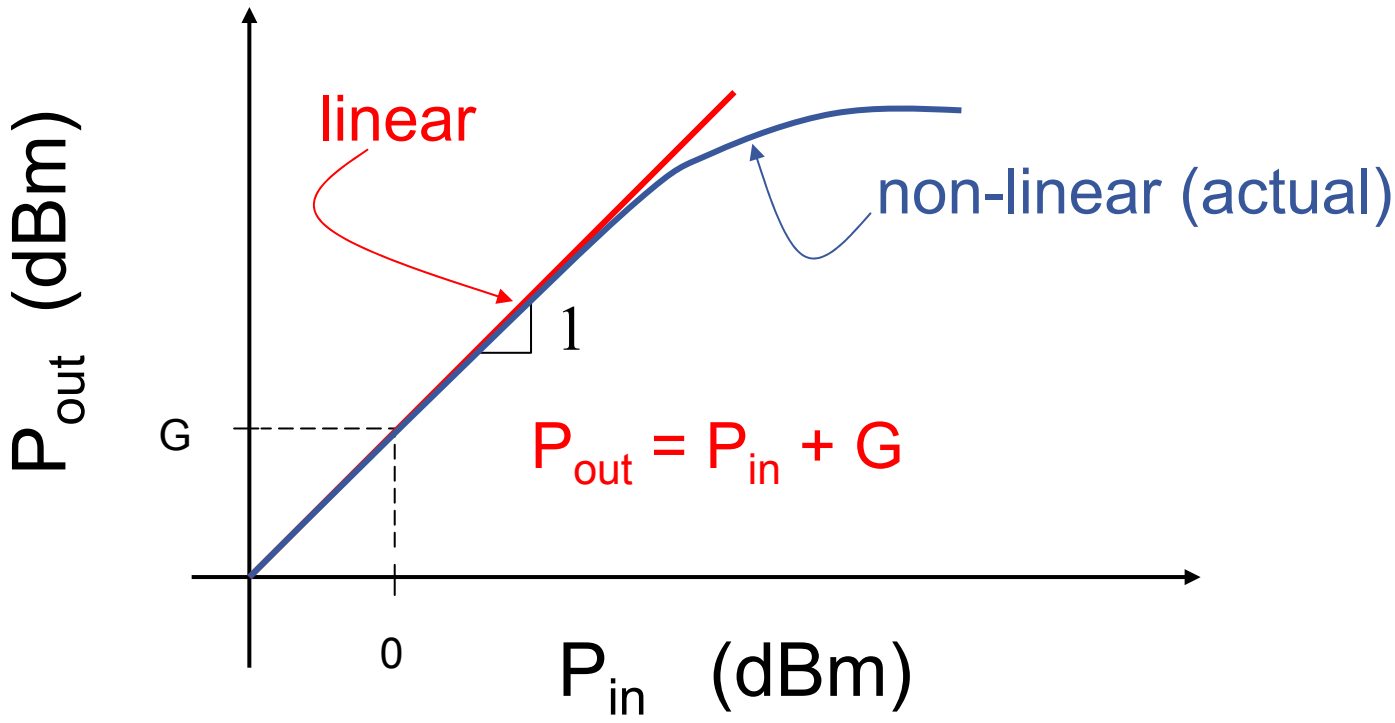
- PA Introduction
  - Power transfer characteristics
  - Intrinsic PA metrics
  - Linear and Non-linear amplifiers
  - PA Architectures
- Single-Stage Linear PA
  - Load-line theory
  - Transistors size
  - Input and Output Matching
  - So why is this so hard?
- High-efficiency PAs
  - Class A, AB, B and C amplifiers

Outline (cont.)

- Real-World Design Example
  - Selecting architecture, number of stages
  - Designing stages
  - Tuning: inter-stage match and output
- System specifications
  - Ruggedness: load mis-match and VSWR
  - Linearity: spectral mask (ACPR), switching transients
  - Noise in receive band
- Power Control

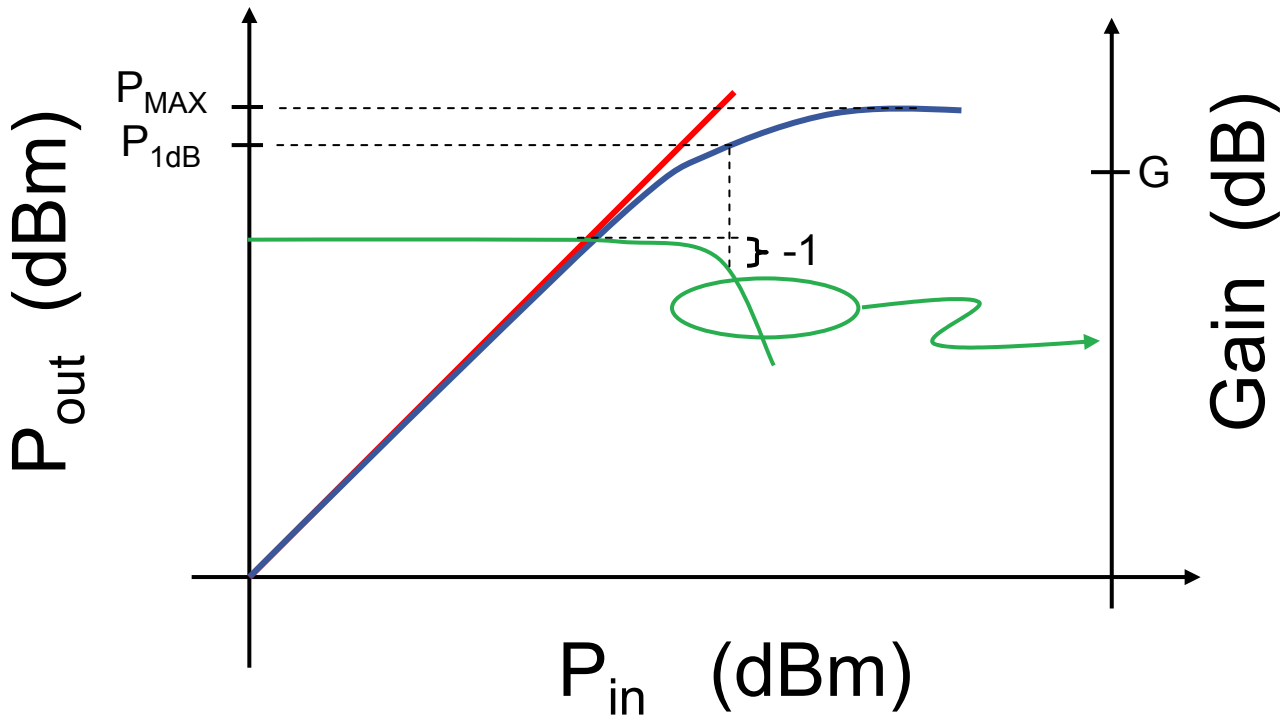
PA Transfer characteristics

Defining linearity:



PA Transfer characteristics

Defining linearity:



PA Introduction: Intrinsic PA Metrics

- **P_{1dB}: Output power at which linear gain has compressed by 1dB (measure of linear power handling)**
- **P_{MAX}: Maximum output power (saturated power)**
- **Gain: Generally taken to mean transducer gain**

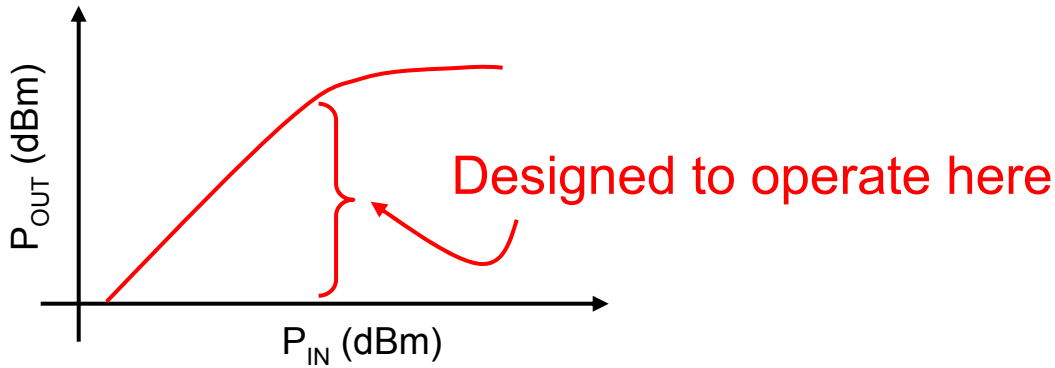
$$\frac{\text{Power delivered to load}}{\text{Power available from source}}$$

- **PAE: Power-added Efficiency**

$$\frac{\text{Power to load} - \text{Power from source}}{\text{Power from supply}}$$

Linear and Non-linear PAs

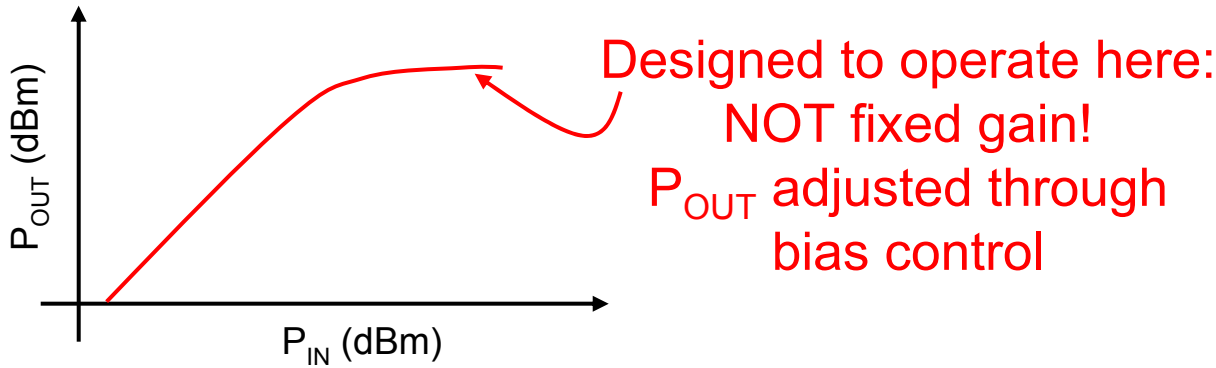
- "Linear PA" generally refers to a PA which operates at constant gain, needs to preserve amplitude information



- Not necessarily class A (will discuss later …) Peak efficiencies often only 40 to 45 %
- Useful for modulation schemes with amplitude modulation (QPSK, 8-PSK, QAM)

Linear and Non-linear PAs

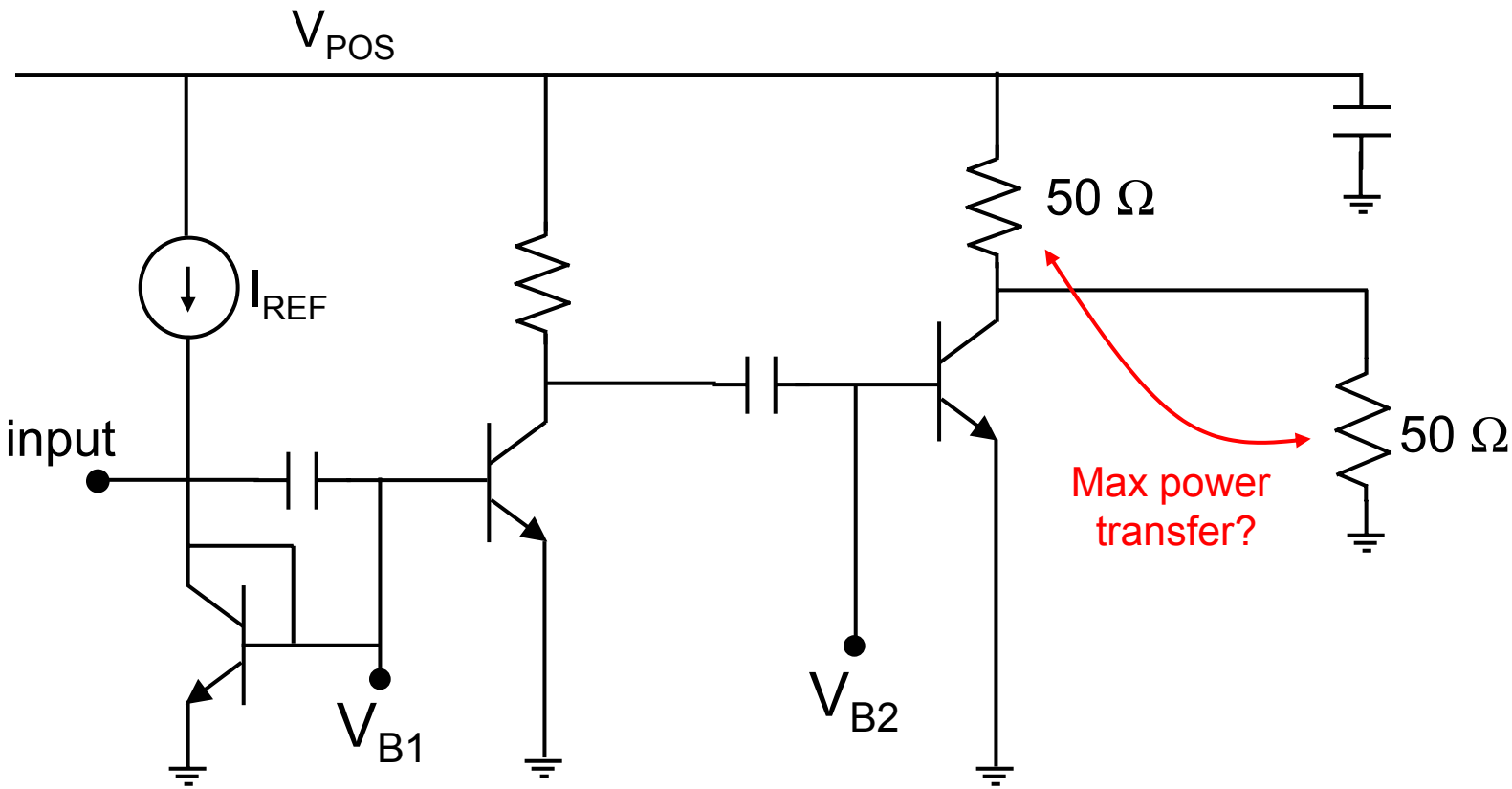
- "Non-linear PA" generally refers to a PA designed to operate with constant P_{IN}, output power varies by changing gain



- Operation in saturated mode leads to high peak efficiencies > 50%; "backed-off" efficiencies drop quickly
- Useful for constant-envelope modulation schemes (GMSK)

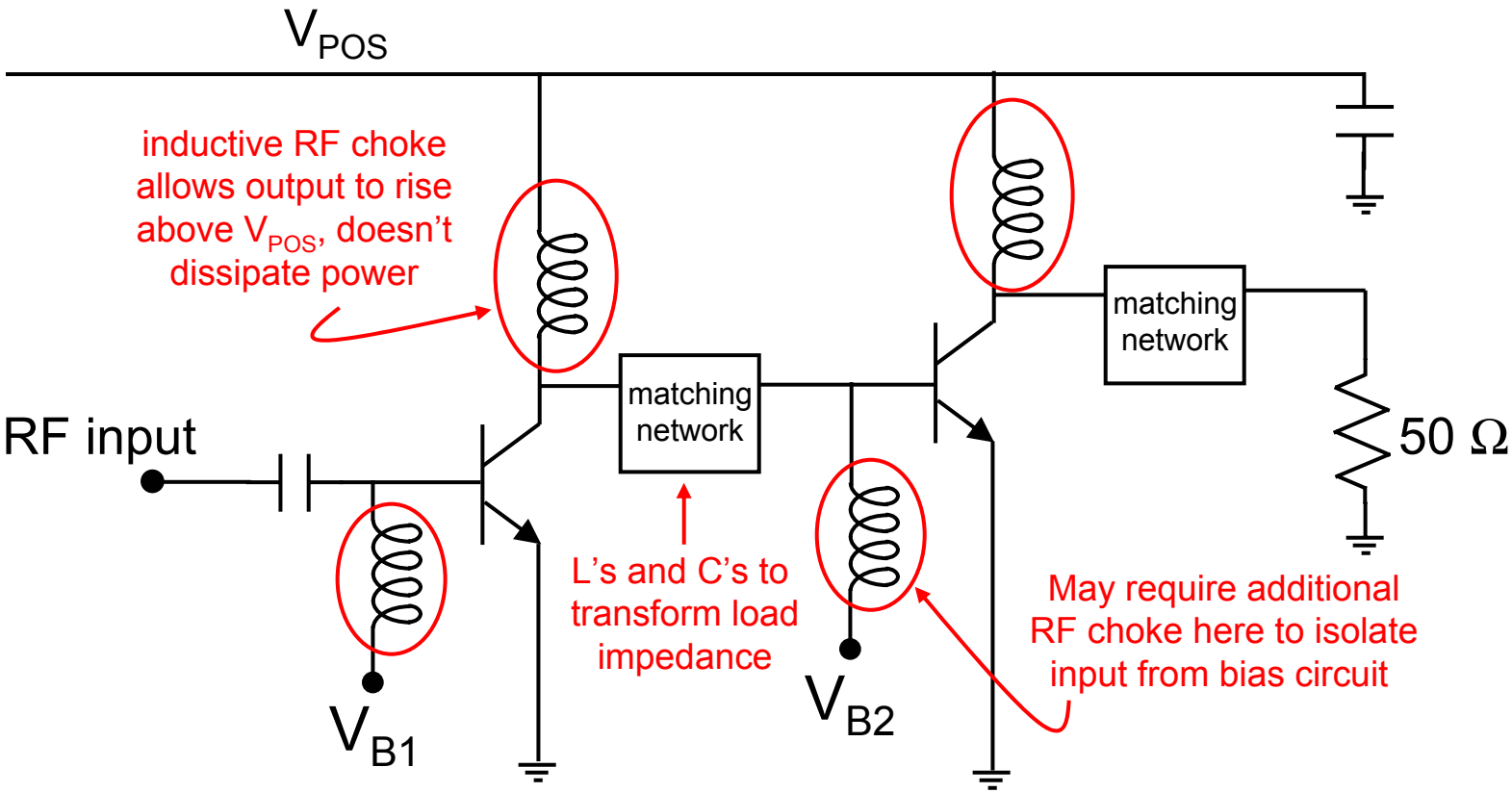
PA Architectures

Typical 2-stage (6.012) design



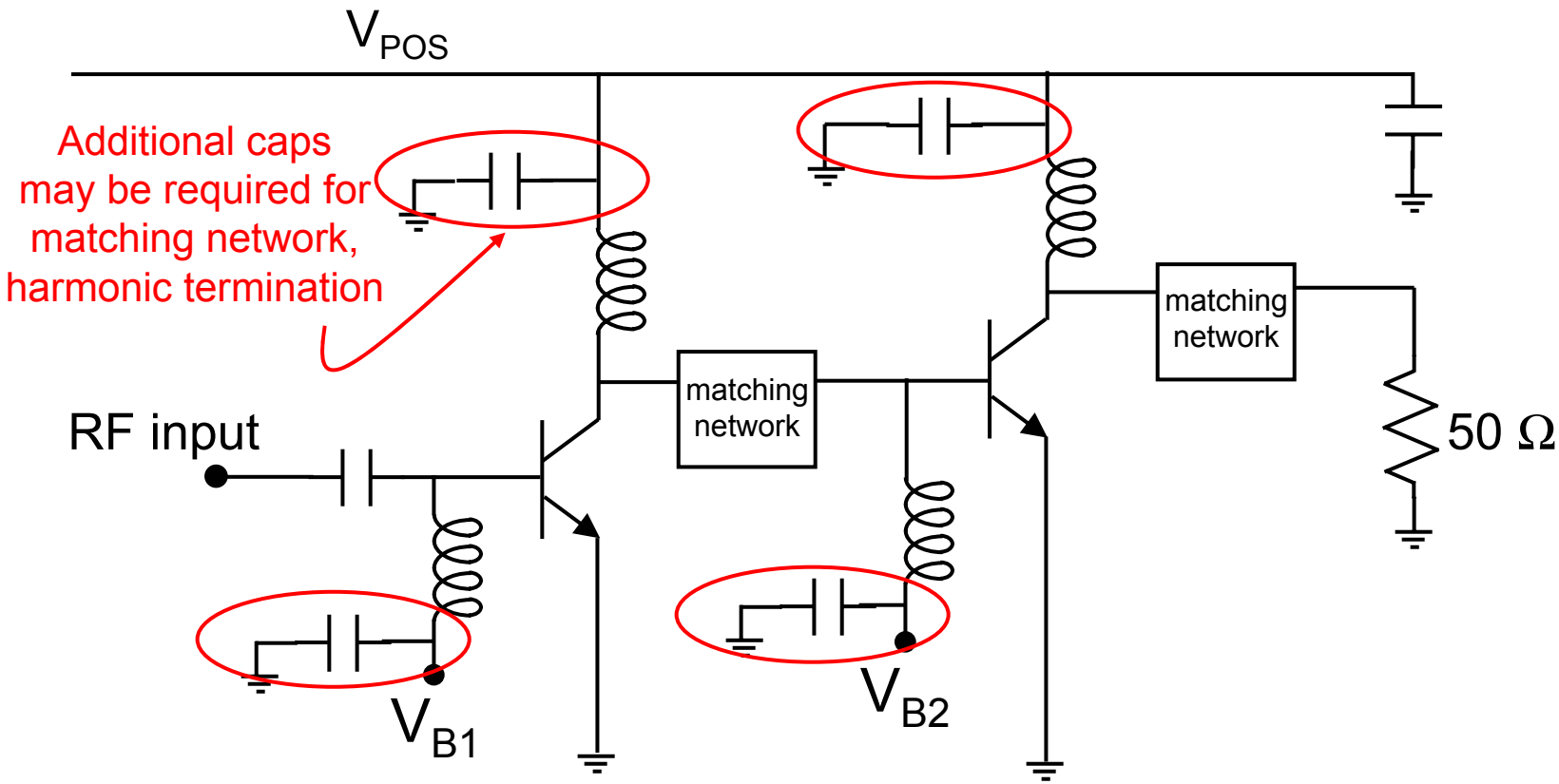
PA Architectures

Typical 2-stage RF PA design



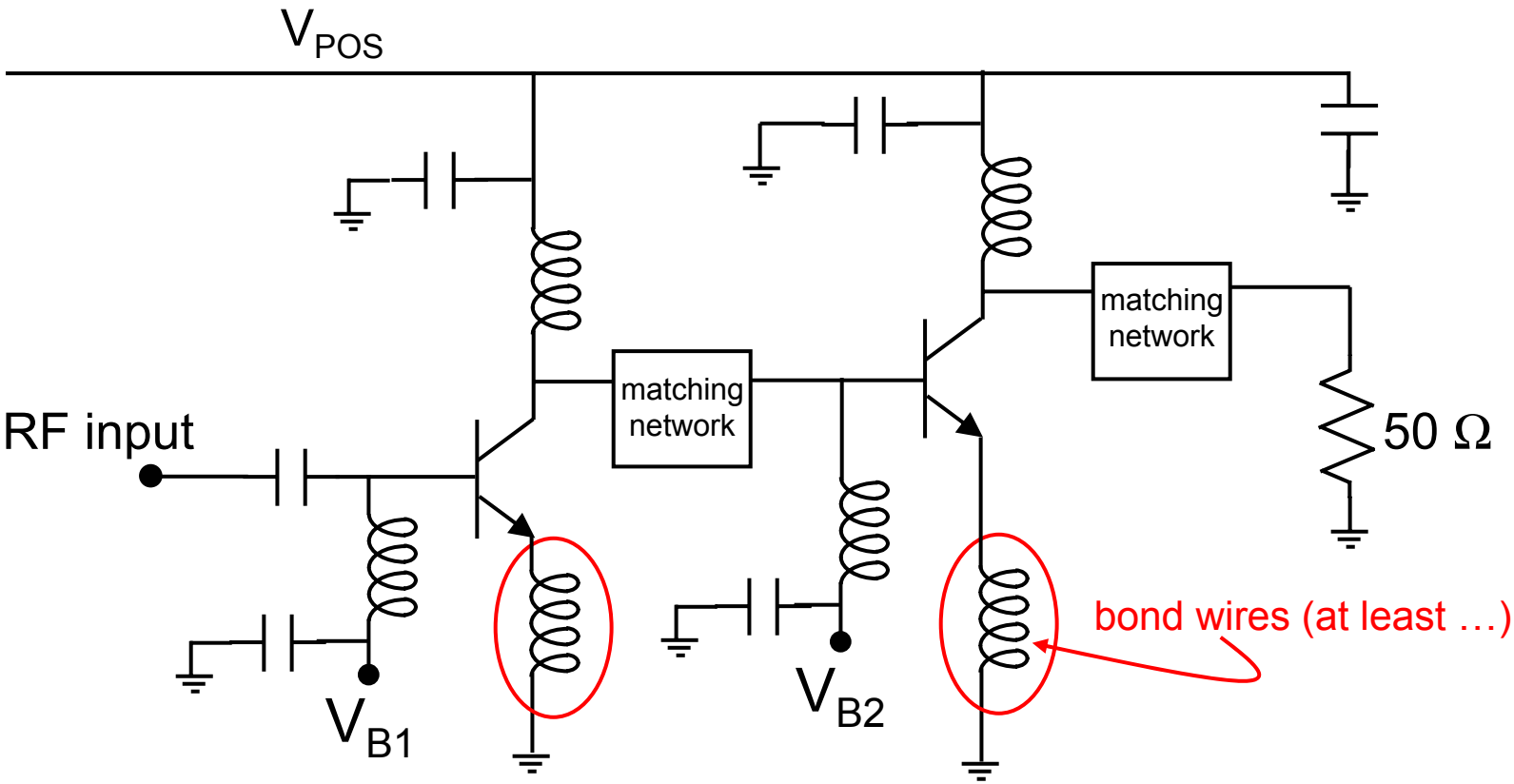
PA Architectures

Typical 2-stage RF PA design



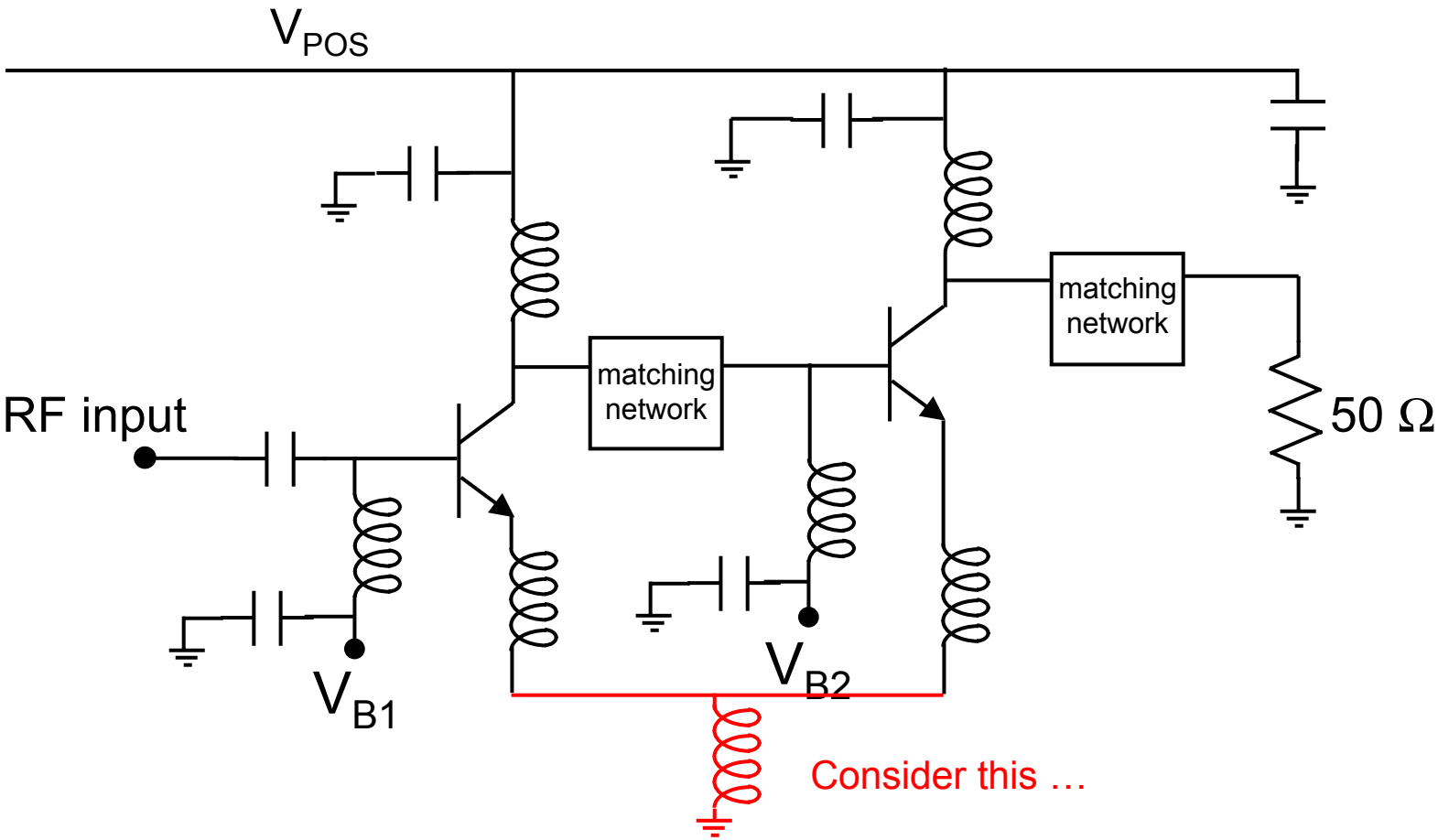
PA Architectures

Typical 2-stage RF PA design



PA Architectures

Typical 2-stage RF PA design

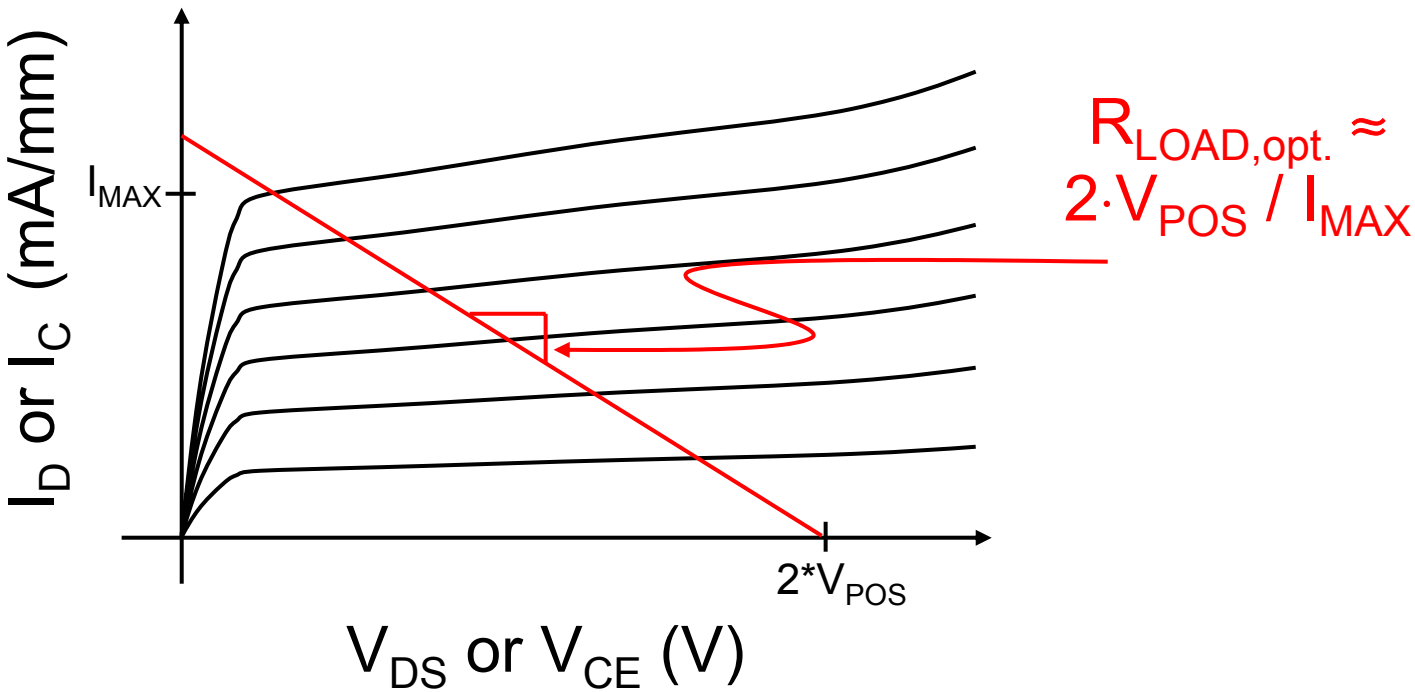


PA Architectures

- "Gain stage" is one transistor with passive elements
- "Active" components often limited to 2 or 3 transistors (gain stages) in signal path
- Transistor design very important!
  - Many parallel transistors – often look like mini-circuits themselves
- Passive components just as important as transistors!
  - Circuits must be tunable to account for uncertainties in determining values *a priori* (i.e. simulations stink – especially large-signal, RF simulations)
  - Q and parasitic elements of passives important

Single-Stage Linear PA

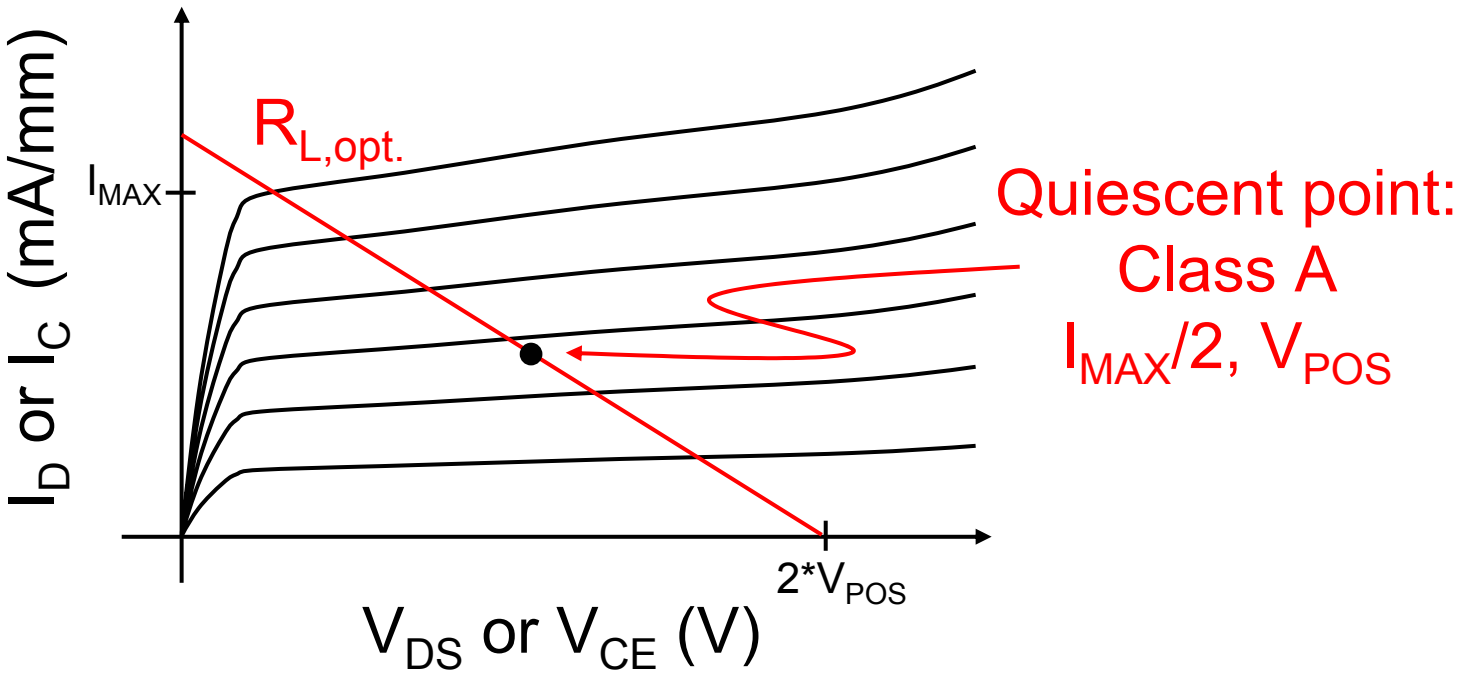
- **Load-line theory: the maximum power that a given transistor can deliver is determined by the power supply voltage and the maximum current of the transistor**



Single-Stage Linear PA

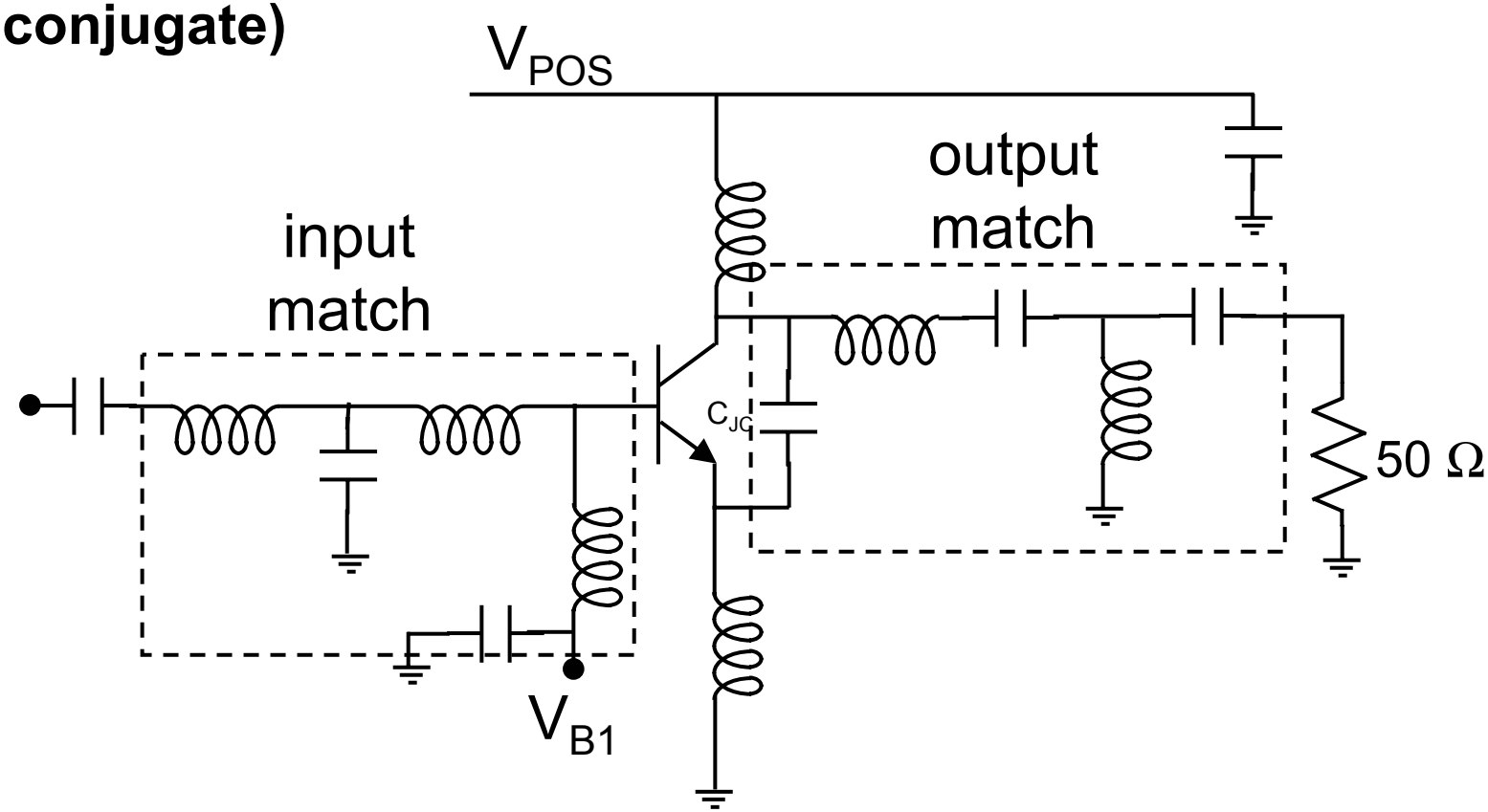
- Transistor size chosen to deliver required output power

$$P_{OUT} \approx I_{MAX} \cdot V_{POS} / 4$$



Single-Stage, Linear PA

- **Design output match to transform 50Ω load to $R_{L,opt}$ at transistor output; then design input match for gain (complex conjugate)**



Seems simple, so why is this so hard?

- Determining I_{MAX} is not so easy
  - For BJTs, one reference suggested that "the best way of estimating its value is to build an optimized class A amplifier and observe the dc supply current."[1]
  - Somewhat easier for depletion-mode GaAs FETs – I_{MAX} often corresponds to V_{GS} = 0V
  - Values don't scale linearly with transistor size
- Optimal load resistance only a theoretical number
  - Transmission line effects, parasitic L's and C's significant at RF
  - Common practice is to vary the load of an actual transistor to determine the peak output power: the load-pull measurement

(Noticing a distinct pattern of "empirical" design emerging?)

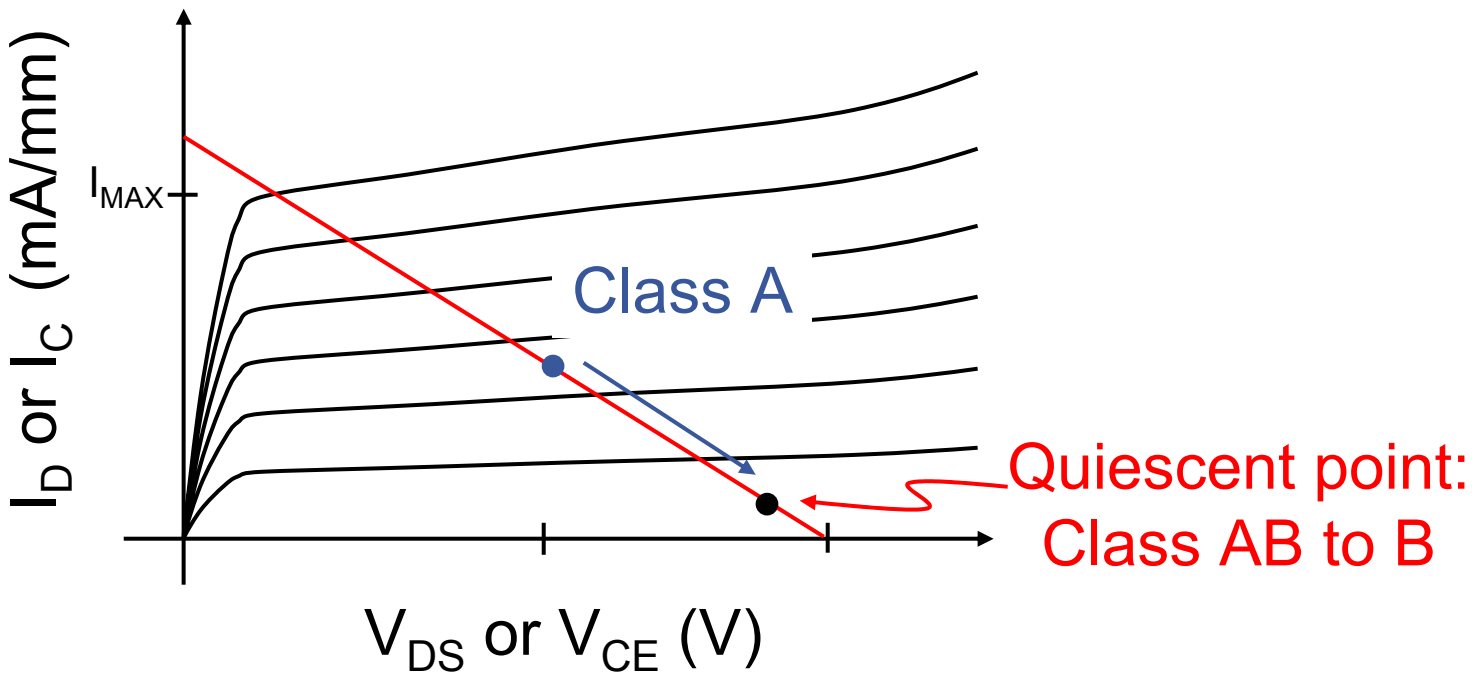
[1] RF Power Amplifiers for Wireless Communications, Steve Cripps, Artech House, Boston, 1999.

Seems simple, so why is this so hard?

- Now consider the problem for multiple stages … double the trouble
  - Typical single-stage gain only 10 – 15 dB
  - Inter-stage match now required to match input impedance of 2nd stage to desired output impedance of 1st stage.
- Problems with matching circuits:
  - Large matching ratios → high Q circuits for simple L matches
  - Multi-segment matches use valuable real estate, add cost
- Transistor itself maters – a lot!
  - Many parallel transistor
  - Ballasting, balancing and layout extremely important

High-efficiency PAs

- Input signal swing turns on transistor – conduction for only part of sinusoidal period



High-Efficiency PAs

- **Assume output match will filter out non-linearities caused by discontinuous conduction:**