Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science

6.035, Fall 2004  
Quiz 3  
Tuesday, November 23

Name:

Please write your name above and at the top of each page. There are 3 questions; you will have 50 minutes to complete the quiz. Please answer as completely and clearly as possible. Illegible or incomprehensible answers will receive little or no credit.

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1. Dominators [25 points]

(a) [15 points]
Recall that a node \( d \) dominates node \( i \) if every path from entry to \( i \) includes \( d \). Draw the dominator tree for the CFG in Figure 1.

(b) [10 points]
In addition to dominators, another useful concept is the postdominator relation. We say that a node \( p \) postdominates node \( i \) if every path from \( i \) to exit includes \( p \). Draw the postdominator tree for the CFG in Figure 1.
Figure 1: Control flow graph for problem 1.
2. Loop Invariant Code Motion [25 points]

For each of the following, state whether or not the statement is loop invariant in the CFG of Figure 2. If a statement is not loop invariant, briefly explain the reason. Assume all variables are live on exit from the loop.

(a) \( q = r + s \)

(b) \( x = y + z \)

(c) \( a = b + c \)

(d) \( i = d + 1 \)

(e) \( d = i + 1 \)
Figure 2: Control flow graph for problem 2.
3. Register Allocation [50 points]

Consider the following function:

```c
int f(int x, int y)
{
    int a, b, c, d, e;

    a = x + 1;
    b = a * 3;
    c = a + b + y;
    b = c;
    d = a / 2;
    for(e=0; e<10; e++) {
        b = b + d;
    }
    c = a + 2;
    return a + b + c + d;
}
```

Assume that variable initializations have been dead-code-eliminated where appropriate.

(a) Draw the def-use chain for the body of this function, and indicate the live range webs.
(b) Draw the interference graph for this function.
(c) Consider a microprocessor with four registers: a stack pointer sp, and the general purpose registers r1, r2, and r3. Suppose that each operation can either use a value from a register or memory, that the calling convention loads x into r1 and y into r2, and returns the function value in r1. Choose the webs with the lowest spill cost to spill. Use a static approximation that assumes loops execute 10 times, and that the cost of a load and store instruction are equivalent. Assign registers to each of the variables in f. State which variables are spilled.
(d) Suppose that the register allocator can split webs and uses a simple greedy heuristic to determine which web to split. Show which webs the allocator would split and draw the new interference graph.