Recitation 13: Propagation Delay, NAND/NOR Gates

Outline

• Propagation Delay for CMOS Inverters
• Why NAND Gate is preferred over NOR Gate?
• Design Project

Propagation Delay for CMOS Inverters

![Figure 1: Discharging cycle: \( t_{\text{PHL}} \), Charging cycle: \( t_{\text{PLH}} \)](image)

Propagation time

\[
\text{Propagation time} = \frac{1}{2}(t_{\text{PLH}} + t_{\text{PHL}})
\]

\[
t = \frac{\text{Charge(toBeCharged/discharged)}}{\text{(Charging/Discharging)Current}}; \quad \text{we treat } C_L \text{ as a linear constant capacitor}
\]

\[
t_{\text{PLH}} = \frac{\frac{1}{2}C_LV_{\text{DD}}}{2L_p\mu_pC_{\text{ox}}(V_{\text{DD}} + V_{T_p})^2}
\]

why \( \frac{1}{2} \)? \( t_p \) is the time to discharge half of initial \( Q \) or charge half of final \( Q \)

\[
t_{\text{PHL}} = \frac{\frac{1}{2}C_LV_{\text{DD}}}{2L_n\mu_nC_{\text{ox}}(V_{\text{DD}} - V_{T_n})^2} = \frac{C_LV_{\text{DD}}}{k_n(V_{\text{DD}} - V_{T_n})^2}
\]

As seen, \( t_p \propto L \). This means, the longer the devices, the slower they become. This gets us to why NAND gates are preferred.
NAND vs. NOR

Gets us to why NAND gates are preferred:

\[ L_{\text{eff}} = 2L_n \]

For symmetrical transfer characteristics,

\[ t_{\text{PLH}} = t_{\text{PHL}} \]
\[ \mu_n = 2\mu_p \]
\[ L_{\text{eff}_n} = 2L_p \]
\[ \therefore w_n = w_p \]

But since \( \mu_n = 2\mu_p \), we are better off having the series connection in NAND (rather than
NOR where PMOS’s are in series). If we wanted the same thing in NOR:

\[
\begin{align*}
\mu_n &= 2\mu_p \\
L_{eff_p} &= 2L_{eff_n} \\
\therefore w_p &= 4w_n
\end{align*}
\]

NOR Structure

So for NAND:

\[
\left( \frac{w}{L} \right)_n = \left( \frac{w}{L} \right)_p \quad \text{Reason is?}
\]

For M-input NAND:

\[
\left( \frac{w}{L} \right)_n = \frac{M}{2} \left( \frac{w}{L} \right)_p
\]

M-input NAND has M-NMOS’s in series \( \implies L_{eff} = ML_n \). So, for \( k_{n_{eff}} = k_{p_{eff}} \):

\[
\begin{align*}
\frac{w_n}{ML_n} \times \mu_n &= \frac{w_p}{L_p} \mu_p \\
\mu_n &= 2\mu_p \\
\frac{w_n}{ML_n} \times 2 &= \frac{w_p}{L_p} \\
\left( \frac{w_n}{L} \right)_n &= \frac{M}{2} \left( \frac{w}{L} \right)_p
\end{align*}
\]
\[ C_L = ? \]

Assume the next stage is another inverter. \( C_L \) is all capacitances seen at node \( V_{out} \).

\[ C_L = C_{\text{g}_{\text{stage2}}} + C_{\text{db}_{p1}} + C_{\text{db}_{n1}} \]

\[ C_{\text{g}_{\text{stage2}}} = C_{\text{g}_{p2}} + C_{\text{g}_{n2}} \]

\[ C_{\text{g}_{n2}} = \frac{2}{3} C_{\text{ox}}(wL)_{n2} + C_{\text{ox}}w_{n2} \approx C_{\text{ox}}(wL)_{n2} \]

\[ C_{\text{db}_{\text{M}}} = C_{\text{j}_{n1}}(wL)_{n2} + C_{\text{j}_{sw_{n1}}}(w + 2L_{\text{diff}})_{n1} \]

\[ \implies C_L = C_{\text{ox}}(wL)_{n2} + C_{\text{ox}}(wL)_{p2} + C_{\text{j}_{n1}}(wL_{\text{diff}})_{n1} + C_{\text{j}_{sw_{n1}}}(w + 2L_{\text{diff}})_{n1} + C_{\text{j}_{p1}}(wL_{\text{diff}})_{p1} + C_{\text{j}_{sw_{p1}}}(w + 2L_{\text{diff}})_{p1} \]
Design Project

What is the use of the circuit? Light in \(\implies\) width modulated electrical signal out.

What does each stage do?

- \(N_1\): charging 1,2 capacitors with \(I_{\text{light}} + I_{\text{bias}}\)

- At \(T_M\): tipping point, \(V_{\text{out}}\) changes from High to Low

\[\implies\text{say} \ V_{M,1} = 1 \text{ V} \]
\[\ V_{M,2} = 2 \text{ V}\]

- Final stage: driver stage
  You need enough current to be able to charge \(C_L\) quickly enough to meet \(t_r\) and \(t_f\) of specs. Decide how many stages you need (remember \(V_{\text{out}}\) positive pulse we need), and think about ratio of sizing between stages (hint: between 3 – 6 is the answer)
Specifications

- $V_{out}$: $t_r, t_f$ 3 ns

- Minimum gate areas

- At least 20 ns distinction between pulse widths corresponding to different $I_{light}$ levels of 0, 1, 2, 3, $\mu$A

- Report: what should you submit

Q & A about design problem