3.155J/6.152J Lecture 2: 
IC Lab Overview

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9/12/2005
Outline

- The MOSFET Structure
- Semiconductor Doping
- The MOSFET as a Switch
- A MOSFET Process
- The MOS Capacitor Process
- Recommended reading
  - Plummer, Chapters 1 and 2
N-Channel MOSFET

- Gate
- Oxide
- n-type
- p-type

$V_G^+$

$0 \, V$

$V_D^+$
A Word About Doping….

Silicon has four valence electrons

It covalently bonds with 4 adjacent atoms in the crystal lattice
Intrinsic Semiconductor

Increasing Temperature Causes Creation of Free Carriers

$10^{10}$ cm$^{-3}$ free carriers at 23C (out of $2 \times 10^{23}$ cm$^{-3}$)

Intrinsic Conductivity
N-type Doping

Phosphorus has 5 valence electrons
‘Donates’ one conduction electron – \textit{n-type}

\textit{Our substrate has} $10^{15}$ \textit{cm}^3 \textit{phosphorus} (1 in $10^8$)

\[
\begin{array}{cccccc}
\text{Si} & \text{Si} & \text{Si} & \text{Si} & \text{Si} & \text{P} \\
\text{Si} & \text{Si} & \text{Si} & \text{Si} & \text{Si} & \\
\text{Si} & \text{Si} & \text{Si} & \text{Si} & \text{Si} & \\
\text{Si} & \text{Si} & \text{Si} & \text{Si} & \text{Si} & \\
\text{Si} & \text{Si} & \text{Si} & \text{Si} & \text{Si} & \\
\end{array}
\]
P-type Doping

Boron has 3 valence electrons
‘Accepts’ one electron from lattice
Creates a ‘hole’ – \( p \)-type
Counter Doping

The addition of one more B than P causes the doping type to change from n-type to p-type.
Counter Doping Process

n-type ($10^{15}$ cm$^{-3}$)

Implant Boron and Anneal

p-type (> $10^{15}$ cm$^{-3}$)

n-type ($10^{15}$ cm$^{-3}$)
P/N Junction

p-type

Depletion Region

n-type

p-type

n-type
P/N Junction - Diode

![Diagram of a diode showing p-type and n-type regions with voltage and current relationships.](image-url)
N-Channel MOSFET Operation

[Diagram showing N-Channel MOSFET operation with symbols and voltages indicated.]
MOSFET as a Switch

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Microfabricated Devices

- Starting Material
  - Single crystal silicon

- Mask Set
  - Contains x,y info
    (Top View)

- Process Sequence
  - Contains z info
    (Cross Section)
Sample Mask Set

Four Levels (Masks)

<table>
<thead>
<tr>
<th>Mask</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Active Area</td>
</tr>
<tr>
<td>2</td>
<td>Polysilicon</td>
</tr>
<tr>
<td>3</td>
<td>Contact Cuts</td>
</tr>
<tr>
<td>4</td>
<td>Aluminum</td>
</tr>
</tbody>
</table>

Transistor (MOSFET)  
Diffusion Resistor (Diode)  
Polysilicon Resistor  
Metal Resistor
Our Process

Poly Gate pMOS

Polycrystalline Silicon

Source

Gate

Drain

Metal-Oxide-Semiconductor (MOSFET)

polysilicon

n-silicon

p-channel

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Starting Material

- 6” (150mm) Diameter Silicon Wafer
  - 30 +/- 1 mil thick (~750 µm)
  - n-type (doped with Phosphorus)
    - 1.5 Ω-cm resistivity (10^{15} cm^{-3} Phos)
  - <100> crystal orientation
FET Process Steps

1. Characterize the wafer (resistivity, orientation, and type)
2. Grow 5000A ‘Field Oxide’ for device isolation

Typically at 800-1100C for 1 hour in O$_2$ or steam
Process Steps

3. Pattern Active Area (Mask #1)

- Coat with photoresist
- Expose
- Develop
- Etch*
- Strip resist

*Wet etch
Process Steps
Process Steps

4. Grow 500A Gate Oxide

5. Deposit 5000A Polysilicon by LPCVD (low pressure chemical vapor deposition)
Process Steps

6. Pattern Polysilicon (Mask #2)
Process Steps

7. Etch Gate Oxide
8. Ion Implantation of Boron

9. Drive-In (950C in O₂)

Note self alignment
Process Steps

10. Strip Backside
Process Steps

11. Pattern Contact Cuts (Mask #3)
12. Evaporate Aluminum
Process Steps

13. Pattern Aluminum (Mask #4)
14. Sinter (400°C – N₂:H₂)
Process Results

The Four Mask Process Yields

- Resistors
  - Metal
  - Polysilicon
  - Diffusion

- Capacitors
  - Metal-Silicon
  - Metal-Polysilicon
  - Polysilicon-Silicon
    - Gate Oxide
    - Field Oxide

- Diode
- MOSFET
- Bipolar Junction Transistor (low quality)
Our Labs

Lab Session 1
- 1.1 Lab Safety and Cleanroom Orientation
- 1.2 RCA (ICL RCA)
- 1.3 Gate Oxidation
  - Thermco Atmospheric Furnace (5D-FieldOx)
  - Dry Oxidation, 1000°C 60 minutes
- 1.4 Doped Polysilicon Deposition
  - Thermco LPCVD (6A-Poly)
- 1.5 Anneal
  - Thermco Atmospheric Furnace (5B-Anneal)

Lab Session 2
- 2.1 Measure oxide and polysilicon thickness (UV1280)
- 2.2 Etch oxide in BOE (Buffered Oxide Etch) until de-wet
- 2.3 HMDS, Photoresist Application, Postbake (SSI coater track)
- 2.4 Dry etch backside polysilicon (LAM490B)
- 2.5 Etch backside oxide in BOE until de-wet (OxEtch-BOE)
- 2.6 Strip frontside resist with Matrix System One Stripper (Asher)

Lab Session 3
- 3.1 HMDS, Photoresist Application, Pre-bake (SSI coater track)
- 3.2 Exposure, Development, and Inspection (I-Stepper)
- 3.3 Dry-etch polysilicon (LAM490B)
- 3.4 Strip photoresist with Matrix System One Stripper (Asher)
- T.1 Device characterization: MOS Capacitor
  - Determine oxide capacitance.
  - Determine bulk dopant concentration.
  - Determine fixed interface charge.
- T.2 Sheet resistance measurement: Van der Pauw structure
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1.1 Lab Safety and Cleanroom Orientation

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Lab Session 3 (Testing)

- **T.1 Device characterization: MOS Capacitor**
  - Determine oxide capacitance.
  - Determine bulk dopant concentration.
  - Determine fixed interface charge.

- **T.2 Sheet resistance measurement: Van der Pauw structure**