Lecture 11 - MOSFET (III)

MOSFET Equivalent Circuit Models

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Contents:

1. Low-frequency small-signal equivalent circuit model
2. High-frequency small-signal equivalent circuit model

Reading assignment:

Howe and Sodini, Ch. 4, §4.5-4.6
Key questions

• What is the topology of a small-signal equivalent circuit model of the MOSFET?

• What are the key dependencies of the leading model elements in saturation?
1. Low-frequency small-signal equivalent circuit model

Regimes of operation of MOSFET:

- **Cut-off**:
  \[ I_D = 0 \]

- **Linear**:
  \[ I_D = \frac{W}{L} \mu_n C_{ox} (V_{GS} - \frac{V_{DS}}{2} - V_T) V_{DS} \]

- **Saturation**:
  \[ I_D = I_{D_{sat}} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda (V_{DS} - V_{DS_{sat}})] \]

Effect of back bias:

\[ V_T(V_{BS}) = V_{To} + \gamma (\sqrt{-2\phi_p} - V_{BS} - \sqrt{-2\phi_p}) \]
Small-signal device modeling

In many applications, interested in response of device to a small-signal applied on top of bias:

Key points:

- Small-signal is small
  ⇒ response of non-linear components becomes linear
- Can separate response of MOSFET to bias and small signal.
- Since response is linear, superposition can be used
  ⇒ effects of different small signals are independent from each other
Mathematically:

\[ i_D(V_{GS} + v_{gs}, V_{DS} + v_{ds}, V_{BS} + v_{bs}) \approx \]

\[
I_D(V_{GS}, V_{DS}, V_{BS}) + \frac{\partial I_D}{\partial V_{GS}}|_Q v_{gs} + \frac{\partial I_D}{\partial V_{DS}}|_Q v_{ds} + \frac{\partial I_D}{\partial V_{BS}}|_Q v_{bs}
\]

where \( Q \equiv \text{bias point} \ (V_{GS}, V_{DS}, V_{BS}) \)

Small-signal \( i_d \):

\[ i_d \approx g_m v_{gs} + g_o v_{ds} + g_{mb} v_{bs} \]

Define:

\( g_m \equiv \text{transconductance} \ [S] \)

\( g_o \equiv \text{output or drain conductance} \ [S] \)

\( g_{mb} \equiv \text{backgate transconductance} \ [S] \)

Then:

\[ g_m \approx \frac{\partial I_D}{\partial V_{GS}}|_Q \quad g_o \approx \frac{\partial I_D}{\partial V_{DS}}|_Q \quad g_{mb} \approx \frac{\partial I_D}{\partial V_{BS}}|_Q \]
Transconductance

In saturation regime:

\[ I_D = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda (V_{DS} - V_{DS_{sat}})] \]

Then (neglecting channel length modulation):

\[ g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_Q \approx \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T) \]

Rewrite in terms of \( I_D \):

\[ g_m = \sqrt{2 \frac{W}{L} \mu_n C_{ox} I_D} \]
Transconductance of $3 \mu m$ nMOSFET ($V_{DS} = 2 V$):

Equivalent circuit model representation of $g_m$:

\[ g_m = \frac{\partial I_d}{\partial V_{gs}} \]

\[ V_{gs} \]
□ Output conductance

In saturation regime:

\[ I_D = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 \left[ 1 + \lambda (V_{DS} - V_{DS_{sat}}) \right] \]

Then:

\[ g_o = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{Q} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 \lambda \simeq \lambda I_D \propto \frac{I_D}{L} \]

Output resistance is inverse of output conductance:

\[ r_o = \frac{1}{g_o} \propto \frac{L}{I_D} \]
Output conductance of 3 \( \mu m \) nMOSFET:

Equivalent circuit model representation of \( g_o \):
\[ I_D \simeq \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2 \]

Then:

\[ g_{mb} = \frac{\partial I_D}{\partial V_{BS}} \bigg|_Q = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T) \left(- \frac{\partial V_T}{\partial V_{BS}} \bigg|_Q \right) \]

Since:

\[ V_T(V_{BS}) = V_{To} + \gamma (\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p}) \]

Then:

\[ \frac{\partial V_T}{\partial V_{BS}} \bigg|_Q = -\frac{\gamma}{2\sqrt{-2\phi_p - V_{BS}}} \]

All together:

\[ g_{mb} = \frac{\gamma g_m}{2\sqrt{-2\phi_p - V_{BS}}} \]

\( g_{mb} \) inherits all dependencies of \( g_m \)
Body of MOSFET is a true gate: output characteristics for different values of $V_{BS}$ ($V_{BS} = 0 - (-3) \, V$, $\Delta V_{BS} = -0.5 \, V$, $V_{GS} = 2 \, V$):

Equivalent circuit model representation of $g_{mb}$:

\[ g_{mb} V_{bs} \]

\[ G \quad V_{gs} \quad S \quad V_{bs} \quad B \]

\[ i_{d} \quad D \]
Complete MOSFET small-signal equivalent circuit model for low frequency:
2. High-frequency small-signal equivalent circuit model

Need to add capacitances. In saturation:

\[ C_{gs} \equiv \text{intrinsic gate capacitance} + \text{overlap capacitance, } C_{ov} \text{ (+fringe)} \]

\[ C_{gd} \equiv \text{overlap capacitance, } C_{ov} \text{ (+fringe)} \]

\[ C_{gb} \equiv \text{(only parasitic capacitance)} \]

\[ C_{sb} \equiv \text{source junction depletion capacitance} + \text{sidewall (+channel-substrate capacitance)} \]

\[ C_{db} \equiv \text{drain junction depletion capacitance} + \text{sidewall} \]

(Items in brackets of second order; will neglected in 6.012)
Complete MOSFET high-frequency small-signal equivalent circuit model:

\[
\begin{align*}
G & \quad C_{gd} \quad D \\
v_{gs} & \quad C_{gs} \quad g_{m}v_{gs} \\
S & \quad C_{sb} \quad g_{mb}v_{bs} \\
v_{bs} & \quad C_{db}
\end{align*}
\]

Plan for development of capacitance model:

- Start with \( C'_{gs,i} \)
  - compute gate charge \( Q_G = -(Q_N + Q_B) \)
  - compute how \( Q_G \) changes with \( V_{GS} \)
- Add pn junction capacitances
Inversion layer charge in saturation

\[ Q_N(V_{GS}) = W \int_0^L Q_n(y) \, dy = W \int_{V_{GS}-V_T}^{V_{GS}} Q_n(V_c) \frac{dy}{dV_c} \, dV_c \]

But:

\[ -E_y(y) = \frac{dV_c}{dy} = -\frac{I_D}{W \mu_n Q_n(V_c)} \]

Then:

\[ Q_N(V_{GS}) = -\frac{W^2L\mu_n}{I_D} \int_{0}^{V_{GS}-V_T} Q_n^2(V_c) \, dV_c \]

Remember:

\[ Q_n(V_c) = -C_{ox}(V_{GS} - V_c - V_T) \]

Then:

\[ Q_N(V_{GS}) = -\frac{W^2L\mu_nC_{ox}^2}{I_D} \int_{0}^{V_{GS}-V_T} (V_{GS} - V_c - V_T)^2 \, dV_c \]
Do integral, substitute $I_D$ in saturation and get:

$$Q_N(V_{GS}) = -\frac{2}{3}WLC_{ox}(V_{GS} - V_T)$$

Gate charge:

$$Q_G(V_{GS}) = -Q_N(V_{GS}) - Q_{B,max}$$  \[\text{independent of } V_{GS}\]

Intrinsic gate-to-source capacitance:

$$C_{gs,i} = \frac{dQ_G}{dV_{GS}} = \frac{2}{3}WLC_{ox}$$

Must add overlap capacitance:

$$\boxed{C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ov}}$$

Gate-to-drain capacitance - only overlap capacitance:

$$C_{gd} = WC_{ov}$$
Body-to-source capacitance = source junction capacitance:

\[ C_{sb} = C_j + C_{jsw} = WL_{diff} \left( \frac{q\epsilon_s N_a}{2(\phi_B - V_{BS})} + (2L_{diff} + W)C_{JSW} \right) \]

Body-to-drain capacitance = drain junction capacitance:

\[ C_{db} = C_j + C_{jsw} = WL_{diff} \left( \frac{q\epsilon_s N_a}{2(\phi_B - V_{BD})} + (2L_{diff} + W)C_{JSW} \right) \]

inner sidewall charge of junctions part of \( C_{jsw} \)
Key conclusions

High-frequency small-signal equivalent circuit model of MOSFET:

In saturation:

\[ g_m \propto \sqrt{\frac{W}{L}} I_D \]

\[ g_o \propto \frac{I_D}{L} \]

\[ C_{gs} \propto W L C_{ox} \]